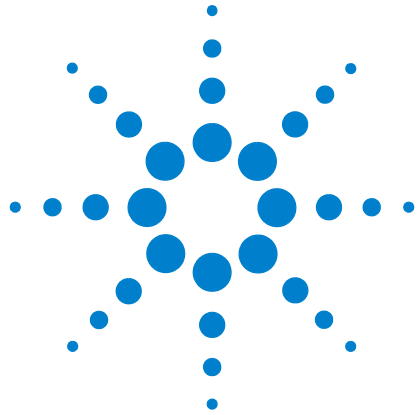




Agilent U7232A DisplayPort Electrical Performance Compliance Test Application

Method of Implementation



Agilent Technologies

Notices

© Agilent Technologies, Inc. 2007-2009

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Agilent Technologies, Inc. as governed by United States and international copyright laws.

Manual Part Number

U7232-97004

Edition

Fifth edition, March 2009

Printed in USA

Agilent Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

Warranty

The material contained in this document is provided “as is,” and is subject to being changed, without notice, in future editions. Further, to the maximum extent permitted by applicable law, Agilent disclaims all warranties, either express or implied, with regard to this manual and any information contained herein, including but not limited to the implied warranties of merchantability and fitness for a particular purpose. Agilent shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein. Should Agilent and the user have a separate written agreement with warranty terms covering the material in this document that conflict with these terms, the warranty terms in the separate agreement shall control.

Technology Licenses

The hardware and/or software described in this document are furnished under a license and may be used or copied only in accordance with the terms of such license.

Restricted Rights Legend

If software is for use in the performance of a U.S. Government prime contract or sub-contract, Software is delivered and licensed as “Commercial computer software” as defined in DFAR 252.227-7014 (June 1995), or as a “commercial item” as defined in FAR 2.101(a) or as “Restricted

computer software” as defined in FAR 52.227-19 (June 1987) or any equivalent agency regulation or contract clause. Use, duplication or disclosure of Software is subject to Agilent Technologies’ standard commercial license terms, and non-DOD Departments and Agencies of the U.S. Government will receive no greater than Restricted Rights as defined in FAR 52.227-19(c)(1-2) (June 1987). U.S. Government users will receive no greater than Limited Rights as defined in FAR 52.227-14 (June 1987) or DFAR 252.227-7015 (b)(2) (November 1995), as applicable in any technical data.

Safety Notices

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

A **WARNING** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a **WARNING** notice until the indicated conditions are fully understood and met.

DisplayPort Automated Testing—At A Glance

The Agilent U7232A DisplayPort Electrical Performance Compliance Test Application helps you verify DisplayPort Source device under test (DUT) compliance to DisplayPort specifications using an Agilent 8 GHz or greater Infiniium digital storage oscilloscope. The DisplayPort Electrical Performance Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE

The tests performed by the DisplayPort Electrical Performance Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

Compliance testing measurements are described in Section 3, Source Compliance Tests, in the *DisplayPort-Compliance Test Specification Version 1.1* document, which complies to the *DisplayPort Standard 1.1a*. For more information, see the VESA web site at www.vesa.org.

Required Equipment and Software

In order to run the DisplayPort automated tests, you need the following equipment and software:

- Version 05.60 or later of Infiniium software (54854A, 54855A and 80000 series Infiniium Digital Storage Oscilloscope) OR
- Version 1.31 or greater of baseline software (90000A series Infiniium Digital Storage Oscilloscope).
- 8 GHz or greater Infiniium Oscilloscope. Option 001 (1 M/ch memory upgrade) is required.
- U7232A DisplayPort Electrical Performance Compliance Test Application version 2.01.
- W2641A DisplayPort Test Point Adapter fixture. Includes four SMA to SMP cables.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable for calibrating the oscilloscope.
- E2655A/B probe de-skew fixture.
- 1168A or 1169A probes and N5380A SMA probe head.
- U7232A DisplayPort Electrical Performance Compliance Test Application license.
- N5400A EZJIT Plus Jitter Analysis software license.

In order to run the DisplayPort source automated tests, you need the following additional hardware:

- W2642A DisplayPort Test Controller (DPTC).
- Quantum Data DisplayPort Adapter.

In This Book

This manual describes the tests that are performed by the DisplayPort Electrical Performance Compliance Test Application in more detail; it contains information from (and refers to) the *DisplayPort Specification Version 1.1*, and it describes how the tests are performed.

- [Chapter 1](#), “Installing the DisplayPort Electrical Performance Compliance Test Application shows how to install and license the automated test application (if it was purchased separately).
- [Chapter 2](#), “Preparing to Take Measurements shows how to start the DisplayPort Electrical Performance Compliance Test Application and gives a brief overview of how it is used.
- [Chapter 3](#), “Source Eye Diagram Differential Tests shows the probing and test procedure of the source data eye diagram differential tests.
- [Chapter 4](#), “Source Total Jitter Differential Tests shows the probing and test procedure of the source total jitter differential tests.
- [Chapter 5](#), “Source Non-ISI Jitter Differential Tests shows the probing and test procedure of the source non-isi jitter differential tests.
- [Chapter 6](#), “Source Transition Time Differential Tests (Informative) describes the source rise time and fall time differential tests. These are informative tests.
- [Chapter 7](#), “Source Non Pre-Emphasis Level Differential Tests describes the source non Pre-Emphasis level differential tests.
- [Chapter 8](#), “Source Overshoot Differential Tests (Informative) shows the probing and test procedure of the source overshoot differential tests. These are informative tests.
- [Chapter 9](#), “Source Pre-Emphasis Level Differential Tests (Normative & Informative) shows the probing and test procedure of the source pre-Emphasis differential tests. The Pre-Emphasis Level tests are normative tests whereas Non-Transition Voltage Range Measurements are informative tests.
- [Chapter 10](#), “Source Inter Pair Skew Differential Tests shows the probing and test procedure of the source inter pair skew differential tests.
- [Chapter 11](#), “Source Unit Interval Differential Tests (Informative) describes the source unit interval differential tests. These are informative tests.
- [Chapter 12](#), “Source Main Link Frequency Compliance Differential Tests shows the probing and test procedure of the source main link frequency compliance differential tests.
- [Chapter 13](#), “Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative) describes the source spread spectrum clocking (SSC) differential tests. In this SSC test, the Modulation

Frequency and Modulation Deviation tests are normative tests whereas Deviation HF Variation tests are informative tests.

- [Chapter 14](#), “Source Rise-Fall Mismatch Single-Ended Tests (Informative) shows the probing and test procedure of the source rise and fall mismatch single-ended tests.
- [Chapter 15](#), “Source Intra Pair Skew Single-Ended Tests shows the probing and test procedure of the source intra pair skew single-ended tests.
- [Chapter 16](#), “Source AC Common Mode Noise Single-Ended Tests shows the probing and test procedure of the source AC common mode noise single-ended tests.
- [Chapter 17](#), “Link Layer Protocol Tests describes the link layer protocol tests.
- [Chapter 18](#), “Sink Eye Diagram Tests shows the probing and test procedure of the sink eye diagram tests.
- [Chapter 19](#), “Sink Total Jitter Tests contains more information on the sink total jitter tests.
- [Chapter 20](#), “Sink Non-ISI Jitter Tests shows the probing and test procedure of the sink non-isi jitter tests.
- [Chapter 21](#), “Cable Eye Diagram Tests shows the probing and test procedure of the cable eye diagram tests.
- [Chapter 22](#), “Cable Total Jitter Tests contains more information on the cable total jitter tests.
- [Chapter 23](#), “Cable Non-ISI Jitter Tests contains more information on the cable non-isi jitter tests.
- [Chapter 24](#), “Calibrating the Infiniium Oscilloscope and Probe describes how to calibrate the oscilloscope in preparation for running the DisplayPort automated tests.
- [Chapter 25](#), “InfiniiMax Probing describes the 1168A/1169A probe amplifier and probe head recommendations for DisplayPort testing.
- [Appendix A](#), “DisplayPort Source Automated Test with W2642A DPTC describes the implementation of test automation features architect in the *DisplayPort Standard Version 1.1a* using Agilent W2642A DisplayPort Test Controller (DPTC).

See Also

- The DisplayPort Electrical Performance Compliance Test Application's online help, which describes:
 - Starting the tests.
 - Creating or opening a test project.
 - Setting up the DisplayPort test environment.
 - Setting up the source automated tests with W2642A DPTC.
 - Selecting tests.
 - Configuring selected tests.
 - Connecting the oscilloscope to the DUT.
 - Running the tests.
 - Viewing the test results.
 - Viewing/printing the HTML test report.
 - Saving test projects.
 - Understanding the HTML report.

Contents

DisplayPort Automated Testing—At A Glance	3
Required Equipment and Software	3
In This Book	5
See Also	7

1 Installing the DisplayPort Electrical Performance Compliance Test Application

Installing the Software	16
Installing the License Key	17

2 Preparing to Take Measurements

W2641A DisplayPort Test Point Adapter Fixture	20
Acquiring the Test Fixture	20
W2641A Test Fixture Description	20
Calibrating the Oscilloscope	21
Starting the DisplayPort Electrical Performance Compliance Test Application	22
Online Help Topics	24

3 Source Eye Diagram Differential Tests

Probing for Source Data Eye Diagram Differential Tests	26
Source Eye Diagram Differential Tests	28
Test Procedure	28
Test Condition	33
PASS Condition	34
Test References	35

4 Source Total Jitter Differential Tests

Probing for Source Total Jitter Differential Tests	38
Source Total Jitter Differential Tests	40
Test Procedure	40
Test Condition	43
PASS Condition	44
Test References	44

5 Source Non-ISI Jitter Differential Tests

Probing for Source Non-ISI Jitter Differential Tests	46
Source Non-ISI Jitter Differential Tests	48
Test Procedure	48
Test Condition	51
PASS Condition	52
Test References	52

6 Source Transition Time Differential Tests (Informative)

Probing for Source Transition Time Differential Tests	54
Source Transition Time Differential Tests	56
Test Procedure	56
Test Condition	59
PASS Condition	59
Test References	60

7 Source Non Pre-Emphasis Level Differential Tests

Probing for Source Non Pre-Emphasis Level Differential Tests	62
Source Non Pre-Emphasis Level Test	64
Test Procedure	64
Test Condition	67
PASS Condition	67
Test References	68

8 Source Overshoot Differential Tests (Informative)

Probing for Source Overshoot Differential Tests	70
Source Overshoot Differential Tests	72
Test Procedure	72
Test Condition	75
PASS Condition	75
Test References	75

9 Source Pre-Emphasis Level Differential Tests (Normative & Informative)

Probing for Source Pre-Emphasis Level Differential Tests	78
--	----

Source Pre-Emphasis Level Differential Tests	80
Test Procedure	80
Test Condition	84
PASS Condition	85
Test References	85

10 Source Inter Pair Skew Differential Tests

Probing for Source Inter Pair Skew Differential Tests	88
Source Inter Pair Skew Differential Test	90
Test Procedure	90
Test Condition	93
PASS Condition	93
Test References	94

11 Source Unit Interval Differential Tests (Informative)

Probing for Source Unit Interval Differential Tests	96
Source Unit Interval Differential Tests	98
Test Procedure	98
Test Condition	101
PASS Condition	101
Test References	102

12 Source Main Link Frequency Compliance Differential Tests

Probing for Source Main Link Frequency Compliance Differential Tests	104
Source Main Link Frequency Compliance Differential Tests	106
Test Procedure	106
Test Condition	109
PASS Condition	109
Test References	109

13 Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)

Probing for Source Spread Spectrum Clocking (SSC) Differential Tests	112
--	-----

Source Spread Spectrum Clocking (SSC) Differential Test	114
Spread Spectrum Modulation Frequency (Normative)	114
Spread Spectrum Modulation Deviation (Normative)	114
Deviation HF Variation (Informative)	114
Test Procedure	115
SSC Modulation Frequency Test Condition	118
SSC Modulation Deviation Test Condition	118
SSC Deviation HF Variation Test Condition	119
SSC Modulation Frequency PASS Condition	119
SSC Modulation Deviation PASS Condition	119
SSC Deviation HF Variation PASS Condition	119
Test References	120

14 Source Rise-Fall Mismatch Single-Ended Tests (Informative)

Probing for Source Rise-Fall Mismatch Single-Ended Tests	122
Source Rise-Fall Mismatch Single-Ended Tests	123
Test Procedure	123
Test Condition	126
PASS Condition	126
Test References	127

15 Source Intra Pair Skew Single-Ended Tests

Probing for Source Intra Pair Skew Single-Ended Tests	130
Source Intra Pair Skew Single-Ended Tests	131
Test Procedure	131
Test Condition	134
PASS Condition	134
Test References	134

16 Source AC Common Mode Noise Single-Ended Tests

Probing for Source AC Common Mode Noise Single-Ended Tests	138
Source AC Common Mode Noise Single-Ended Test	139
Test Procedure	139
Test Condition	142
PASS Condition	143
Test References	143

17 Link Layer Protocol Tests

Probing for Link Layer Protocol Tests	146
---------------------------------------	-----

Link Layer Protocol Tests	147
Link Layer Protocol - Pre-Emphasis	147
Link Layer Protocol - Level	147
Link Layer Protocol - Bit Rate	147
Test Procedure	148
Pre-Emphasis Test Condition	151
Level Test Condition	151
Bit Rate Test Condition	151
Pre-Emphasis PASS Condition	152
Level PASS Condition	152
Bit Rate PASS Condition	152
Test References	152

18 Sink Eye Diagram Tests

Probing for Sink Eye Diagram Tests	154
Sink Eye Diagram Tests	156
Test Procedure	156
PASS Condition	161
Test References	162

19 Sink Total Jitter Tests

Probing for Sink Total Jitter Tests	164
Sink Total Jitter Tests	166
Test Procedure	166
PASS Condition	171
Test References	171

20 Sink Non-ISI Jitter Tests

Probing for Sink Non-ISI Jitter Tests	174
Sink Non-ISI Jitter Tests	176
Test Procedure	176
PASS Condition	181
Test References	182

21 Cable Eye Diagram Tests

Probing for Cable Eye Diagram Tests	184
-------------------------------------	-----

Cable Eye Diagram Tests	186
Test Procedure	186
PASS Condition	191
Test References	192

22 Cable Total Jitter Tests

Probing for Cable Total Jitter Tests	194
Cable Total Jitter Tests	196
Test Procedure	196
PASS Condition	201
Test References	201

23 Cable Non-ISI Jitter Tests

Probing for Cable Non-ISI Jitter Tests	204
Cable Non-ISI Jitter Tests	206
Test Procedure	206
PASS Condition	211
Test References	212

24 Calibrating the Infiniium Oscilloscope and Probe

Required Equipment for Calibration	214
Internal Calibration	215
Probe Calibration and De-skew	219
SMA probe head Atten/Offset Calibration	219
Differential Probe Head Skew Calibration	223
SMA Probe Head Atten/Offset Calibration	224
SMA Probe Head Skew Calibration	229

25 InfiniiMax Probing

A DisplayPort Source Automated Test with W2642A DPTC

Aux Channel and Hot Plug Detect (HPD)	234
DPTC Controller	235
Automated Test Sequence	236
OPTION 1	236
OPTION 2	241

Index



1 Installing the DisplayPort Electrical Performance Compliance Test Application

Installing the Software 16

Installing the License Key 17

If you purchased the U7232A DisplayPort Electrical Performance Compliance Test Application version 2.01, you need to install the software and license key.



Installing the Software

- 1 Make sure you have version 05.60 or higher of the Infiniium oscilloscope software or Version 1.31 or greater of baseline software by choosing **Help>About Infiniium...** from the main menu.
- 2 To obtain the DisplayPort Electrical Performance Compliance Test Application, go to Agilent website:
<http://www.agilent.com/find/scope-apps-sw>.

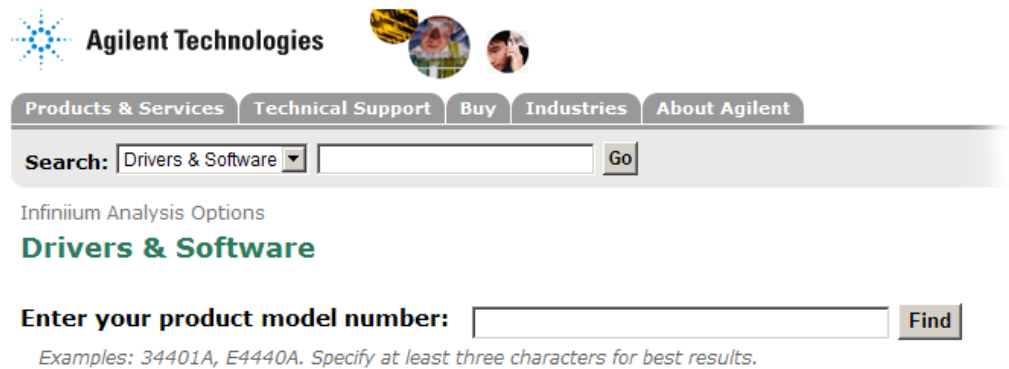


Figure 1 Agilent website for software Downloads

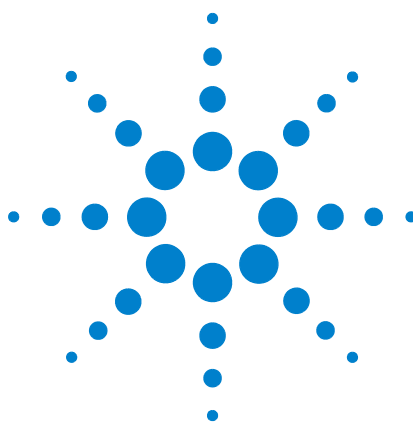
- 3 Search the list on this web page for the link to the U7232A DisplayPort Electrical Performance Compliance Test Application. Click on it and follow the instructions to download and install the application.

Installing the License Key

- 1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.
- 2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**
- 3 In the Install Option License dialog, enter your license code and click **Install License**.
- 4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.
- 5 Click **Close** to close the Install Option License dialog.
- 6 Choose **File>Exit**.
- 7 Restart the Infiniium oscilloscope application to complete the license installation.

1 Installing the DisplayPort Electrical Performance Compliance Test Application



2 Preparing to Take Measurements

W2641A DisplayPort Test Point Adapter Fixture [20](#)

Calibrating the Oscilloscope [21](#)

Starting the DisplayPort Electrical Performance Compliance Test
Application [22](#)

Online Help Topics [24](#)

Before running the DisplayPort automated tests, you need to acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort Electrical Performance Compliance Test Application and perform the measurements.



W2641A DisplayPort Test Point Adapter Fixture

The W2641A test fixture is the Agilent DisplayPort test point adapter fixture that is used for all of the DisplayPort compliance tests.

Acquiring the Test Fixture

The W2641A DisplayPort test point adapter fixture can be acquired from Agilent Technologies.

W2641A Test Fixture Description

Figure 2 shows the top view of the W2641A test fixture.

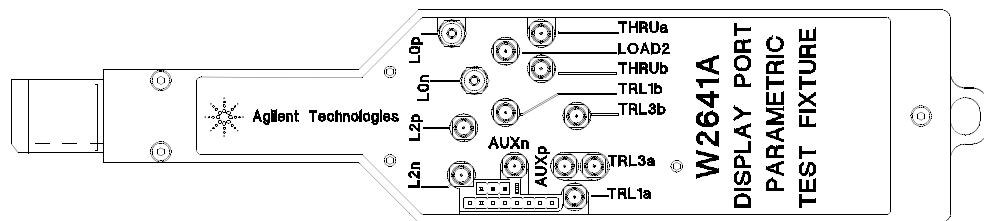


Figure 2 W2641A DisplayPort Test Point Adapter Fixture (Top View)

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see [Chapter 24](#), "Calibrating the Infiniium Oscilloscope and Probe."

NOTE

If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE

If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort Electrical Performance Compliance Test Application

- 1 From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DisplayPort Test**.

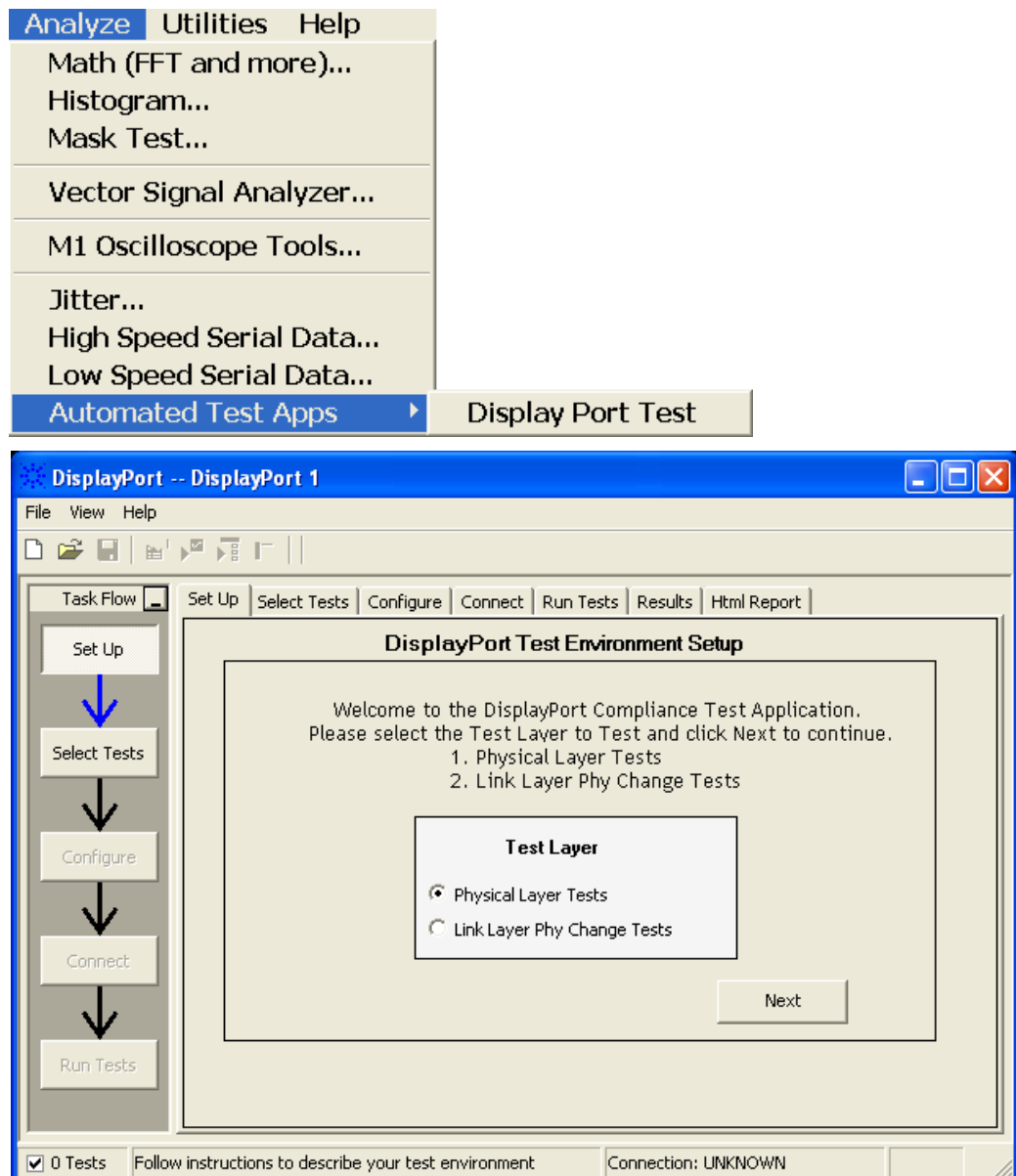


Figure 3 The DisplayPort Electrical Performance Compliance Test Application

NOTE

If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort Electrical Performance Compliance Test Application has not been installed (see [Chapter 1](#), “Installing the DisplayPort Electrical Performance Compliance Test Application”).

[Figure 3](#) shows the DisplayPort Electrical Performance Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you select your setup options. Allows you to setup by connection type, device identifier, jitter separation measurements and test fixture type.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested and configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE

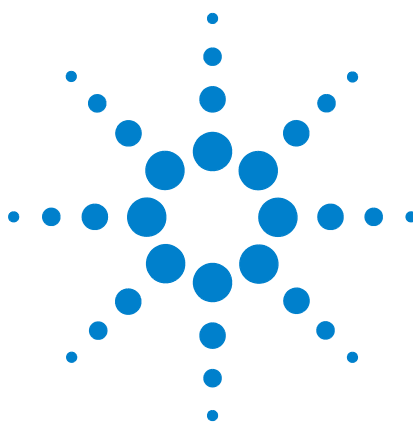
When you close the DisplayPort application, each channel's probe is configured as single-ended or differential depending on the last DisplayPort test that was run.

Online Help Topics

For information on using the DisplayPort Electrical Performance Compliance Test Application, see the online help (which you can access by choosing **Help>Contents...** from the application's main menu).

The DisplayPort Electrical Performance Compliance Test Application's online help describes:

- Running the Compliance Test Application on a second monitor.
- Starting the DisplayPort Electrical Performance Compliance Test Application.
 - To view or minimize the task flow pane.
 - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DisplayPort test environment.
- Setting up DisplayPort automated tests with W2642A DPTC.
- Selecting the tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running the tests.
- Viewing test results.
 - To show reference images and flash mask hits.
 - To change the display settings.
 - To change the margin thresholds and report trial display.
 - To change the auto-recovery option.
- Viewing or printing the HTML test report.
- Saving the test projects.
- Understanding the DisplayPort HTML report.



3

Source Eye Diagram Differential Tests

Probing for Source Data Eye Diagram Differential Tests [26](#)

Source Eye Diagram Differential Tests [28](#)

This section provides the guidelines for source eye diagram differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Data Eye Diagram Differential Tests

When performing the data eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 4 and Figure 5 show a physical connection for making differential and single-ended connections.

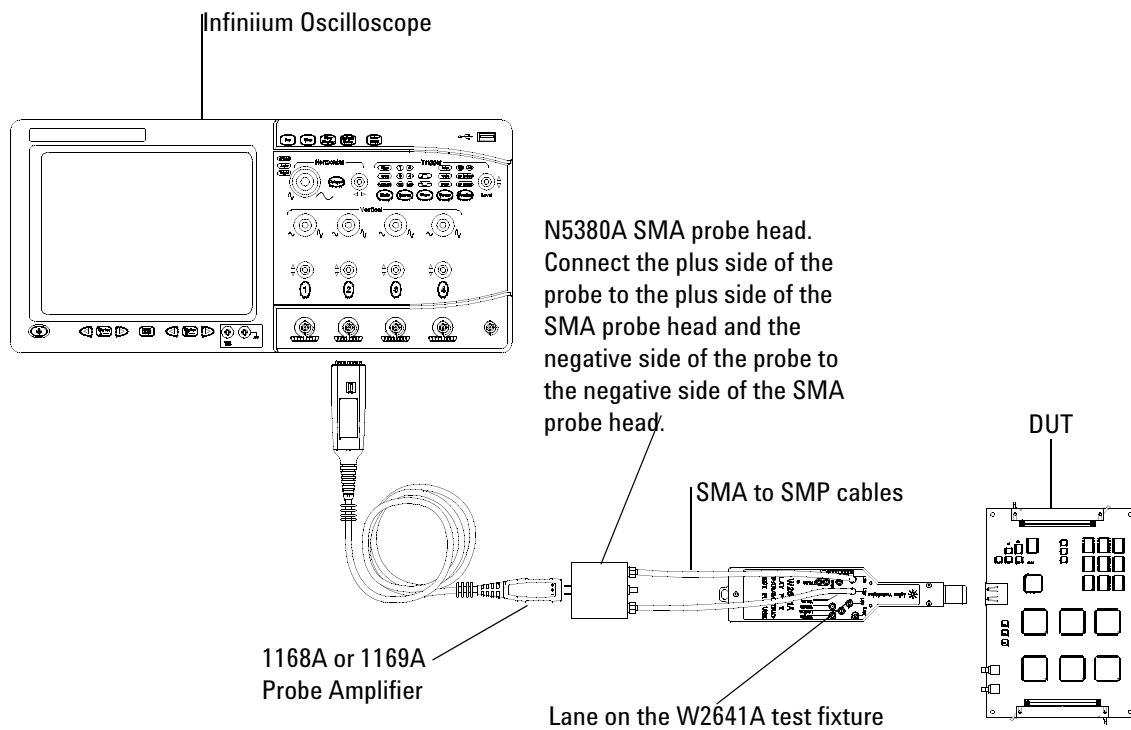


Figure 4 Probing for Differential Tests - Data Eye Diagram Tests (Single Connection with W2641A DisplayPort Test Fixture)

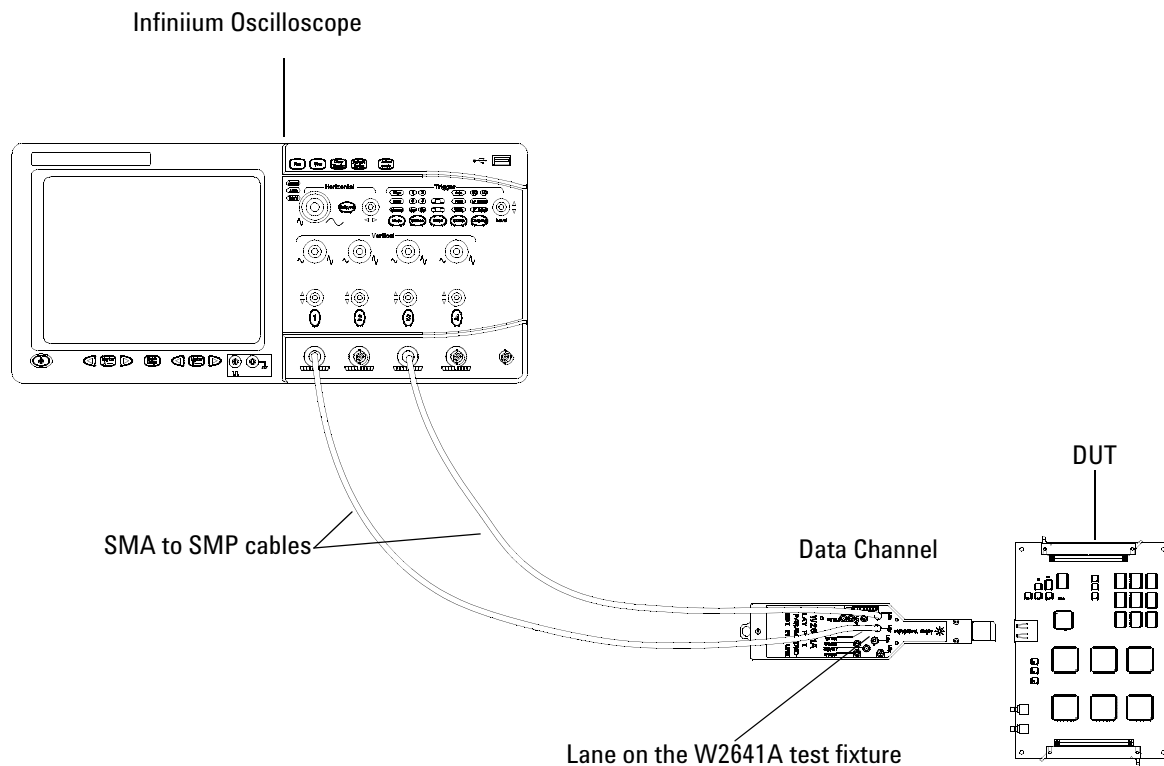


Figure 5 Differential Measurement Setup Using Two Single Ended Connections - Data Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see [Chapter 25](#), “InfiniiMax Probing,” starting on page 231.

Source Eye Diagram Differential Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in transmitted data. The test must use a PRBS 7 test pattern at all voltage levels. The test should be performed without pre-Emphasis.

The source eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.

6 In the DisplayPort Compliance Test Application, click the Set Up tab.

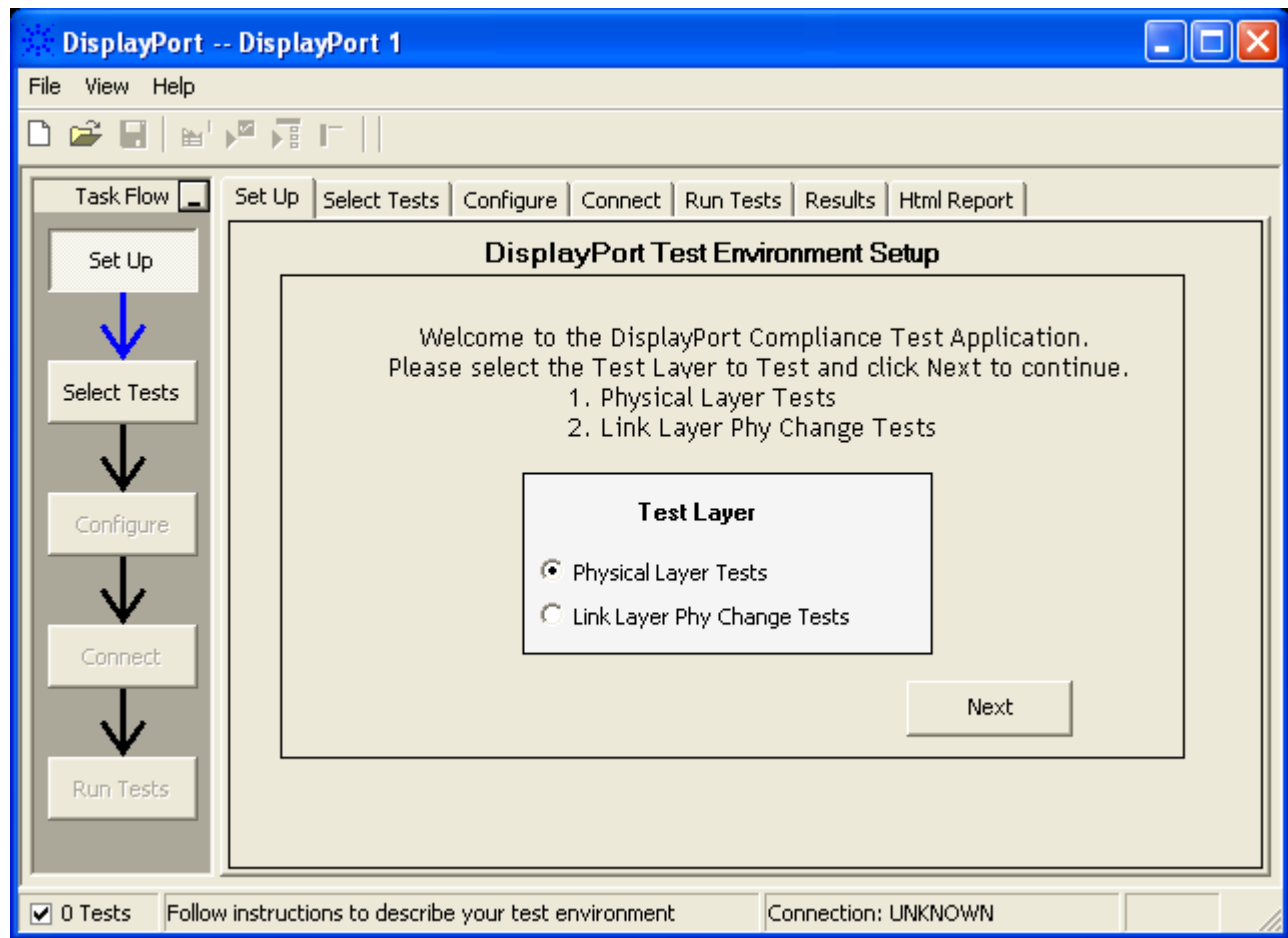


Figure 6 Set Up for Data Eye Pattern Differential Tests

Test Process Setup

Test Mode

☒ Compliance Conditions Only
☐ User Defined Conditions
☐ Targeted Characterization Testing

Description:

Test Mode: DisplayPort Compliance Application allows three Test Modes if Physical Layer Tests is selected

Device Type:

Source

Test Type:

Both

Description:

Device Type: DisplayPort compliance application defines three categories for the type of device (s)

☒ Enable Automation
☒ Hide Informative Tests

<< Back Next >> Close

Figure 7 Test Type Set Up for Data Eye Pattern Differential Tests

- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the Eye Diagram - Lane # - Eye Diagram Test where # is the lane number to be tested.

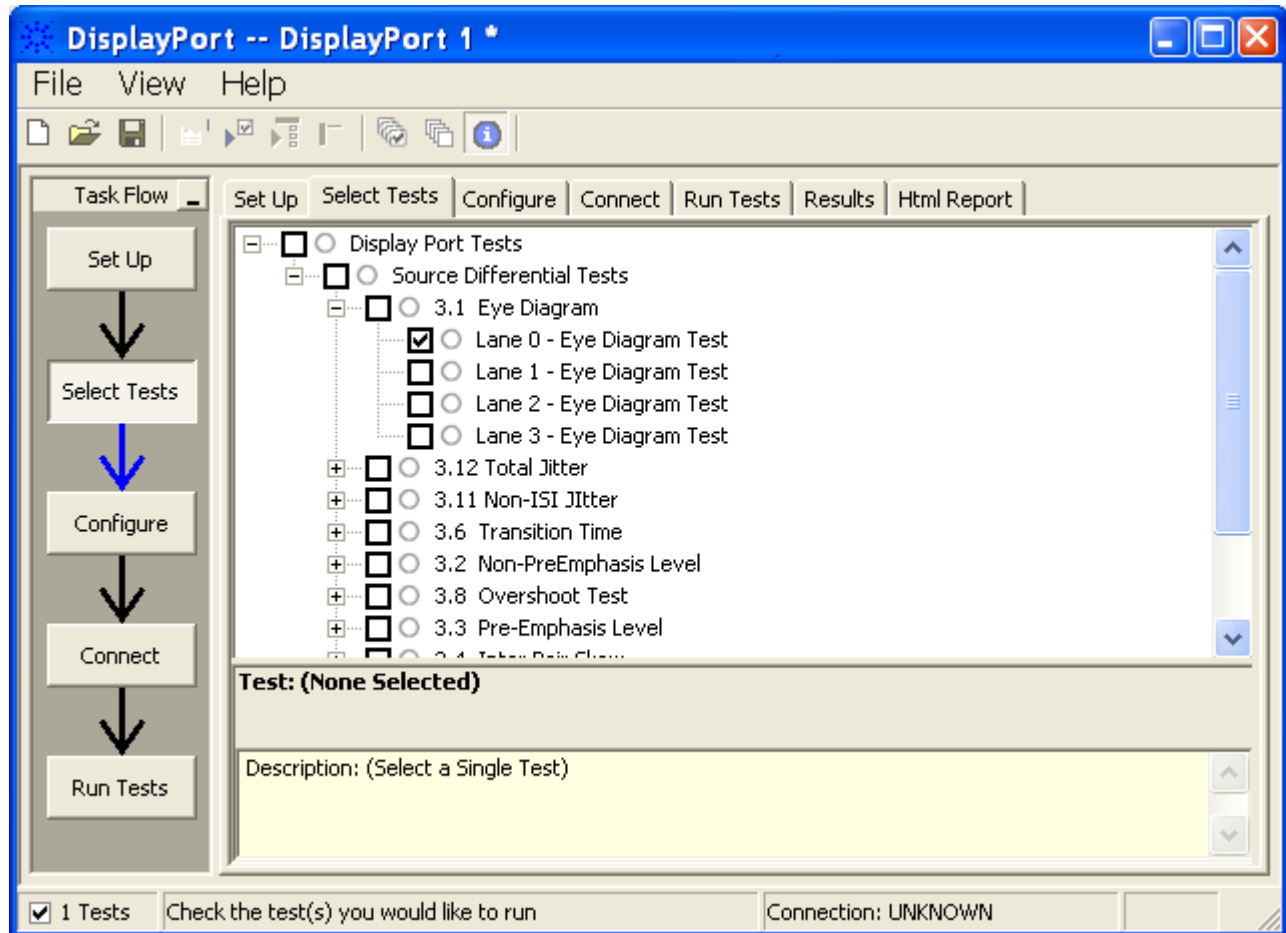


Figure 8 Selecting Data Eye Pattern Differential Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 1](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 1 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 1 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Eye Diagram	
Eye Diagram Edge	Sets the number of edges measured for the eye test.
Mask Scaling Option	Sets the type of scaling performed on the mask for the eye test.
Mask Type	Selects the type of mask to use for the eye test.
Eye Diagram Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
CTS Version for Eye Mask	Set the mask file to CTS version 1.0 or 1.1

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. [Table 2](#) shows the voltage and time coordinates for the mask used in the eye diagram. The specification states that either 400mV, 600mV, or 800mV setting must pass.

Table 2 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.875, 0.000	0.790, 0.000
6	0.709, -0.200	0.645, -0.175
7	0.500, -0.200	0.500, -0.175
8	0.291, -0.160	0.355, -0.140

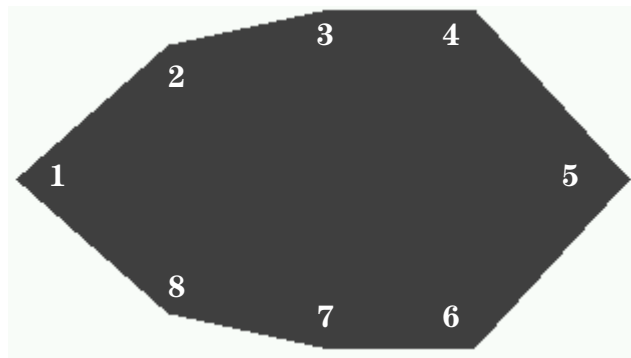


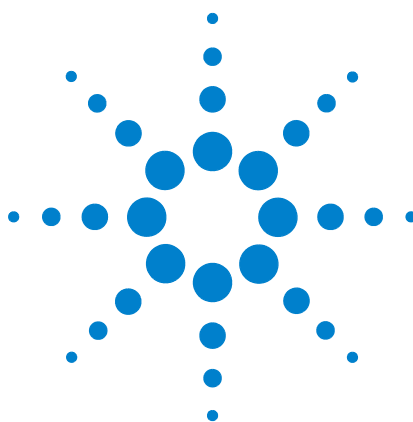
Figure 9 The Source Eye Pattern Mask

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort-Compliance Test Specification Version 1.1*.

3 Source Eye Diagram Differential Tests



4 Source Total Jitter Differential Tests

Probing for Source Total Jitter Differential Tests 38

Source Total Jitter Differential Tests 40

This section provides the guidelines for source total jitter differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Total Jitter Differential Tests

When performing the source total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 10 and Figure 11 show a physical connection for making differential and single-ended connections.

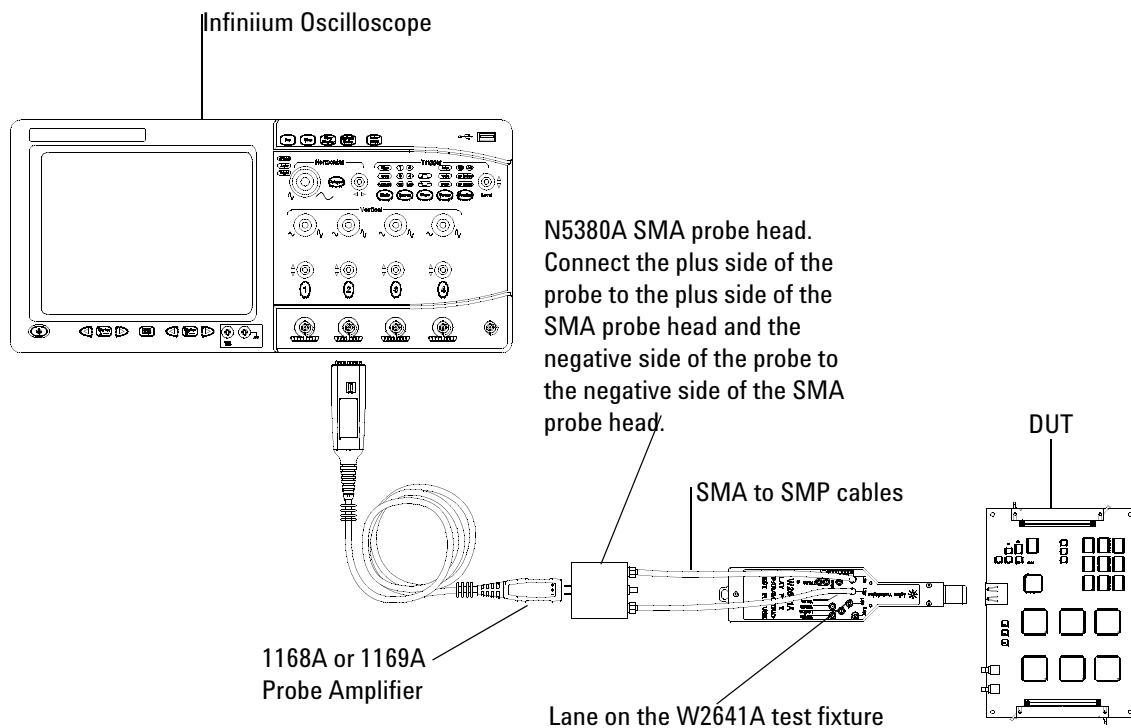


Figure 10 Probing for Differential Tests - Total Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

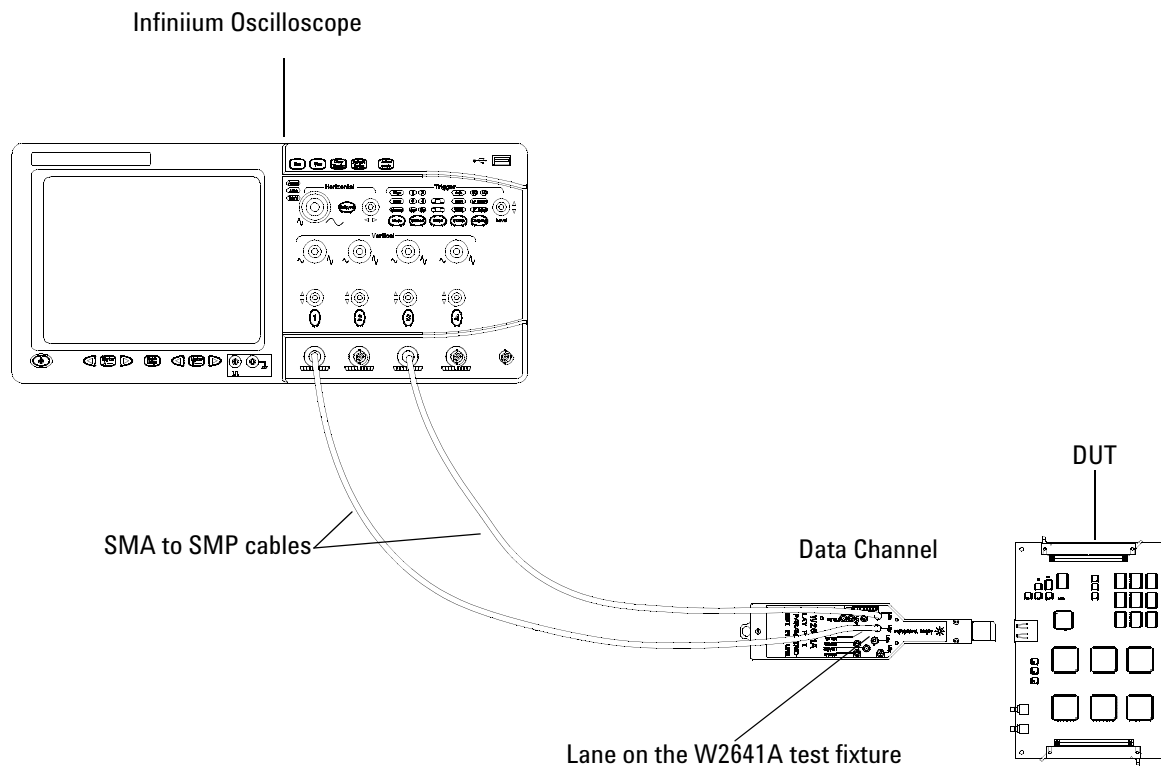


Figure 11 Differential Measurement Setup Using Two Single Ended Connections - Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Total Jitter Differential Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the Total Jitter - Lane # - where # is the lane number to be tested.

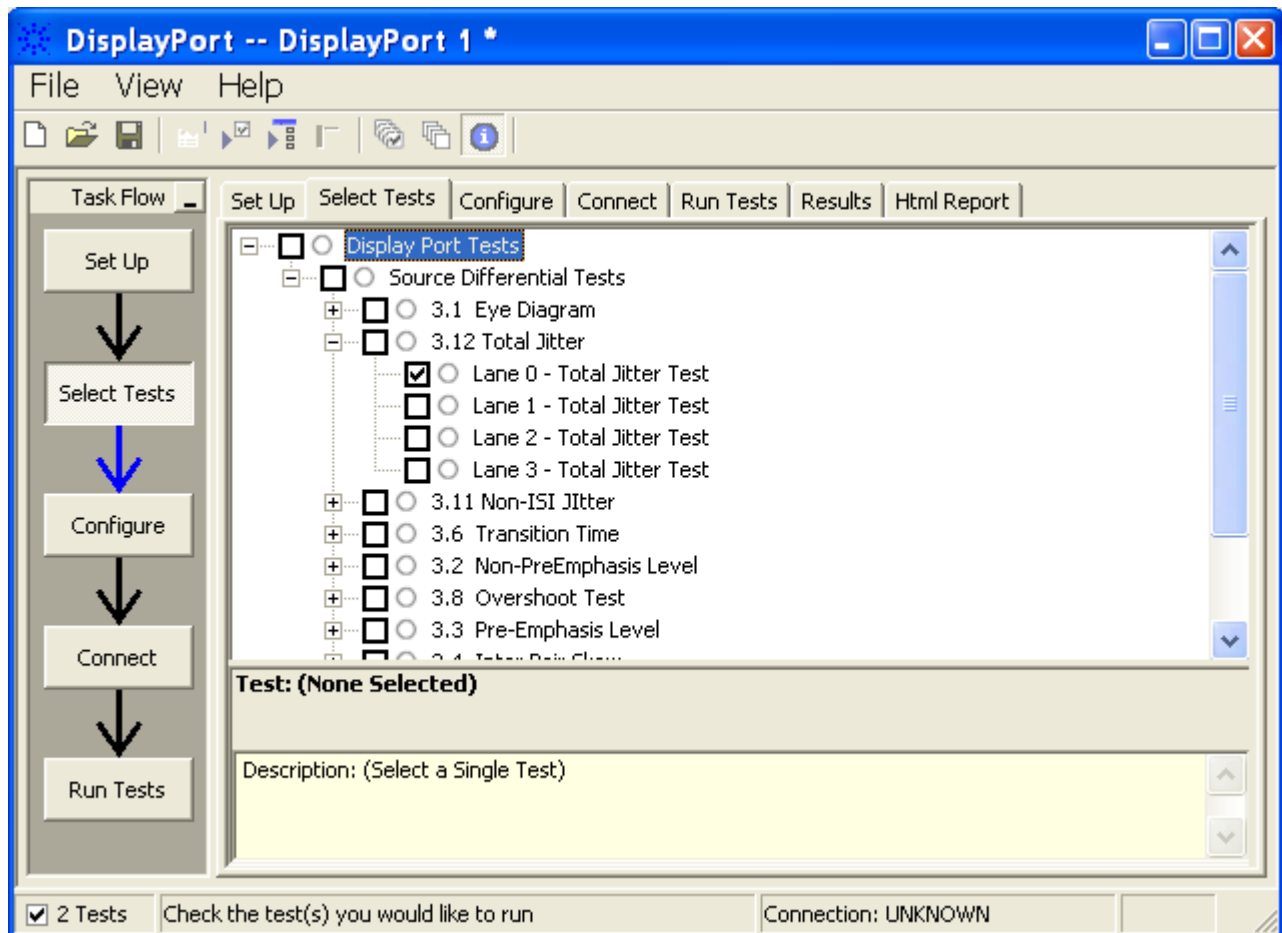


Figure 12 Selecting Source Total Jitter Differential Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 3](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 3 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 3 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

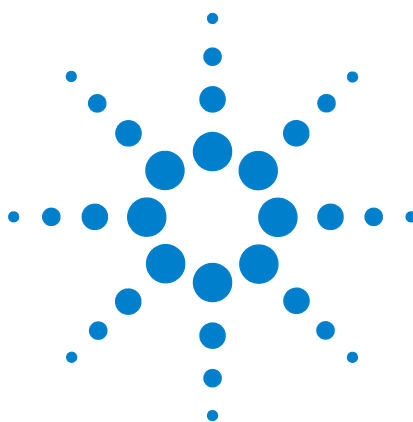
Table 4 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.180 UI	0.254 UI

UI is Unit Interval.

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort-Compliance Test Specification Version 1.1*.



5 Source Non-ISI Jitter Differential Tests

Probing for Source Non-ISI Jitter Differential Tests 46

Source Non-ISI Jitter Differential Tests 48

This section provides the guidelines for source non-ISI jitter differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Non-ISI Jitter Differential Tests

When performing the non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 13 and Figure 14 show a physical connection for making differential and single-ended connections.

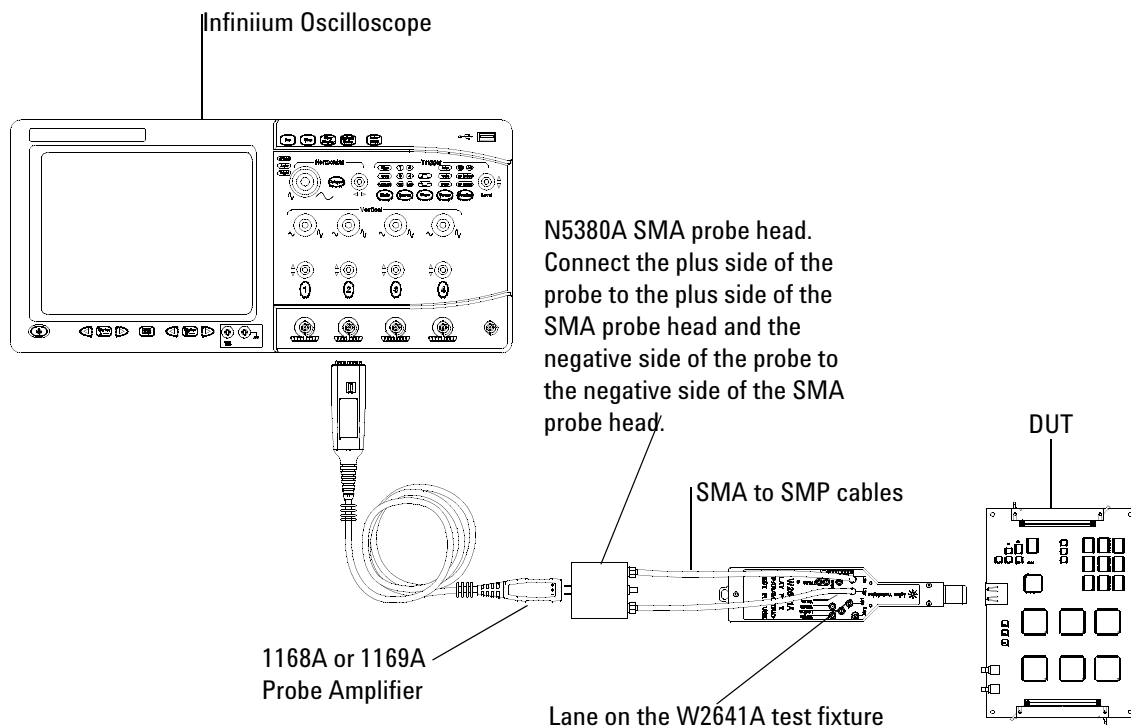


Figure 13 Probing for Differential Tests - Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

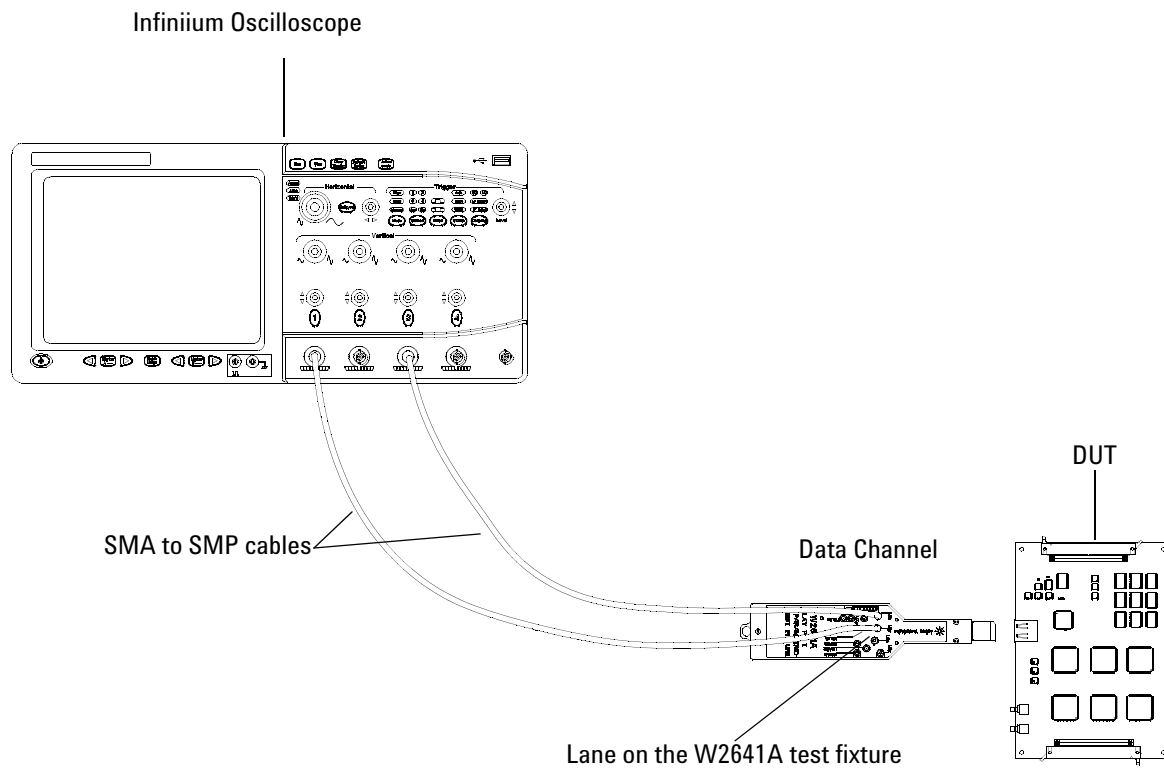


Figure 14 Differential Measurement Setup Using Two Single Ended Connections - Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Non-ISI Jitter Differential Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the Non-ISI Jitter - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

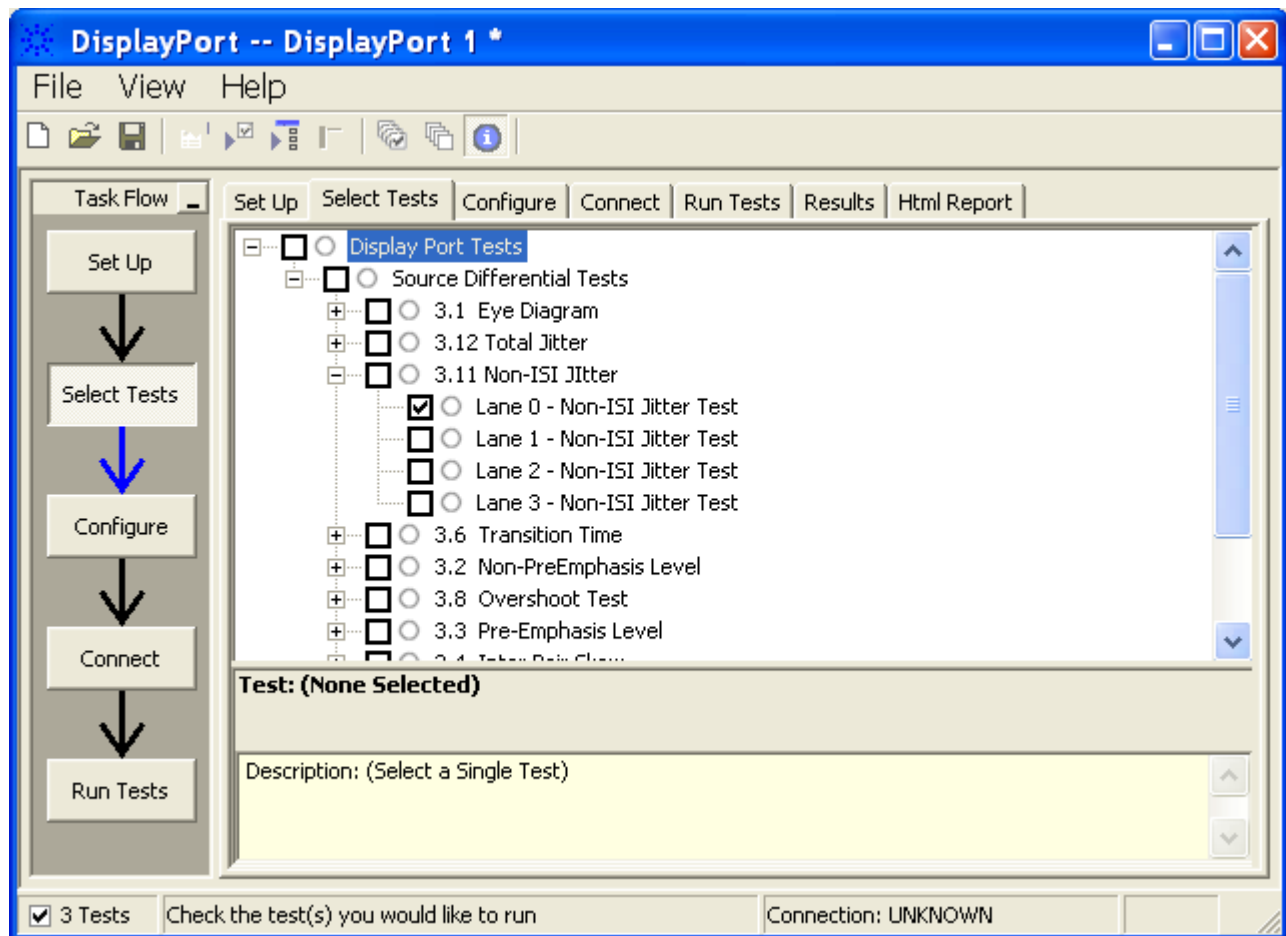


Figure 15 Selecting Source Non-Jitter Differential Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 5](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 5 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 5 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Jitter Separation Settings	
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error rate	Sets the bit error rate for the RJ/DJ measurements.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

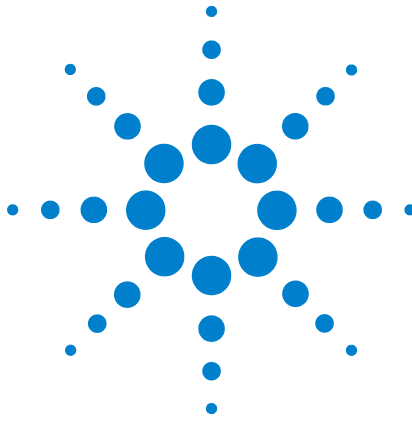
Table 6 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.170 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the *DisplayPort-Compliance Test Specification Version 1.1*.



6 Source Transition Time Differential Tests (Informative)

Probing for Source Transition Time Differential Tests 54

Source Transition Time Differential Tests 56

This section provides the guidelines for source transition time differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Transition Time Differential Tests

When performing the transition time test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 16 and Figure 17 below show the differential and the single-ended connections for Transition Time Differential Tests.

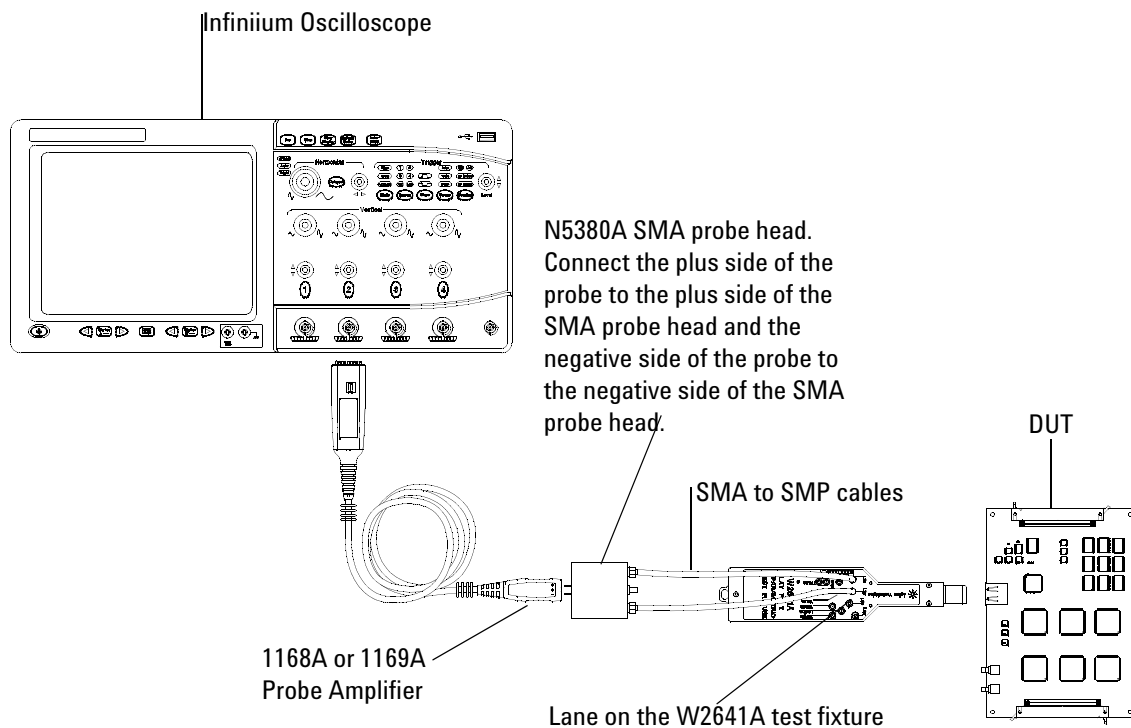


Figure 16 Probing for Differential Tests - Transition Time Tests (Single Connection with W2641A DisplayPort Test Fixture)

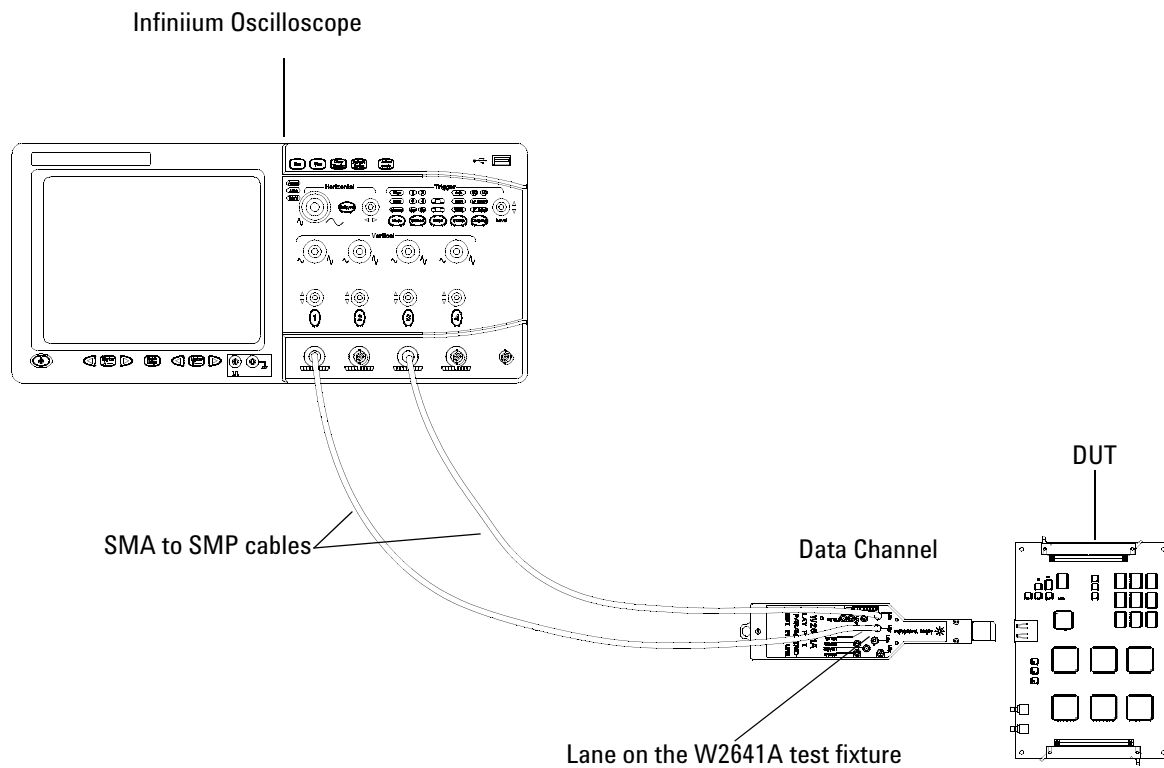


Figure 17 Differential Measurement Setup Using Two Single Ended Connections - Transition Time Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Transition Time Differential Tests

Transition time testing measures the rise time and fall time across the outputs of a differential data lane. The transition is defined as the time interval between the normalized 20% and 80% amplitude levels.

The transition time test should be performed at all bit rates supported without pre-Emphasis for 400 mV differential voltage swing. The source pattern should be a PRBS 7 waveform. This applies to one, two, and four lane operation with all functional lanes being tested. (Reference: Table 3.10 VESA DisplayPort Standard).

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 This is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

Navigate to the Transition Time group, and check the rise time and fall time tests that you want to perform.

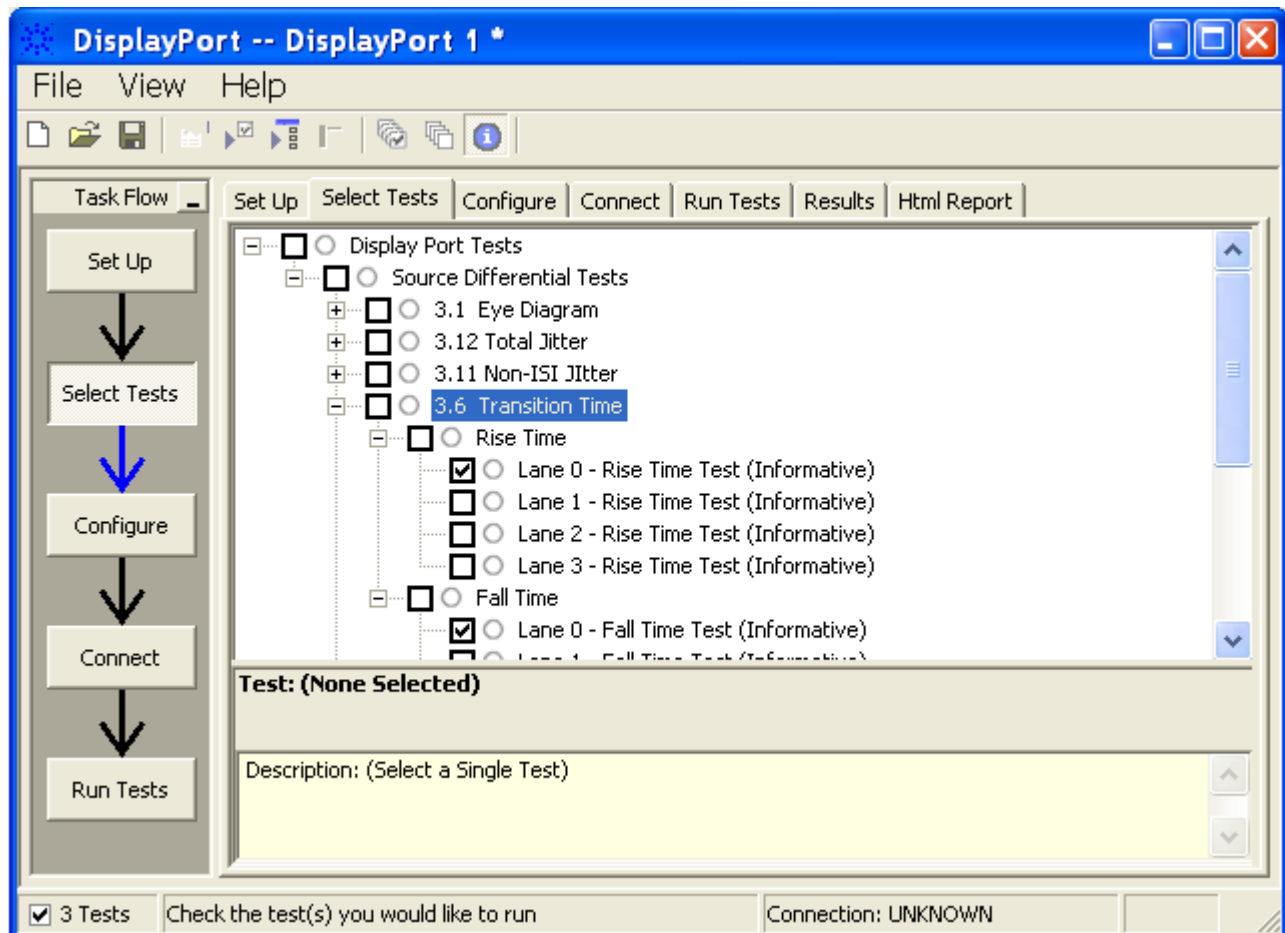


Figure 18 Selecting Transition Time Differential Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 7](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 7 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 7 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Transition Time	
Transition Edges	Sets the number of edges measured for the transition tests.
Transition VH Pattern	Sets the pattern for rise time measurement to either 01111, 0111 or 011. The default setting is 0111.
Transition VL Pattern	Sets the pattern for fall time measurement to either 10000, 1000 or 100. The default setting is 1000.
Threshold	Specifies the threshold in percentage.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

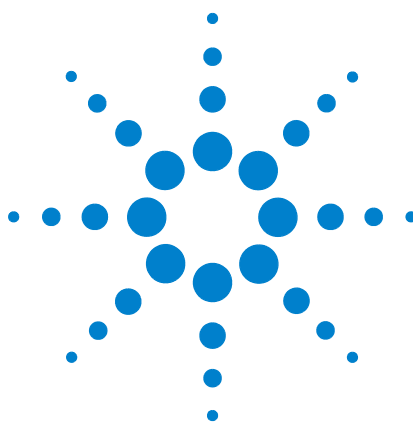
SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

$50 \text{ ps} \leq \text{Transition Time} \leq 160 \text{ ps}$

Test References

See section 3.6, in the *DisplayPort- Compliance Test Specification Version 1.1*.



7 Source Non Pre-Emphasis Level Differential Tests

Probing for Source Non Pre-Emphasis Level Differential Tests [62](#)

Source Non Pre-Emphasis Level Test [64](#)

This section provides the guidelines for source non pre-Emphasis level differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Non Pre-Emphasis Level Differential Tests

When performing the non pre-Emphasis level differential test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 19 and Figure 20 below show the differential and the single-ended connections for Non Pre-Emphasis Level Differential Tests..

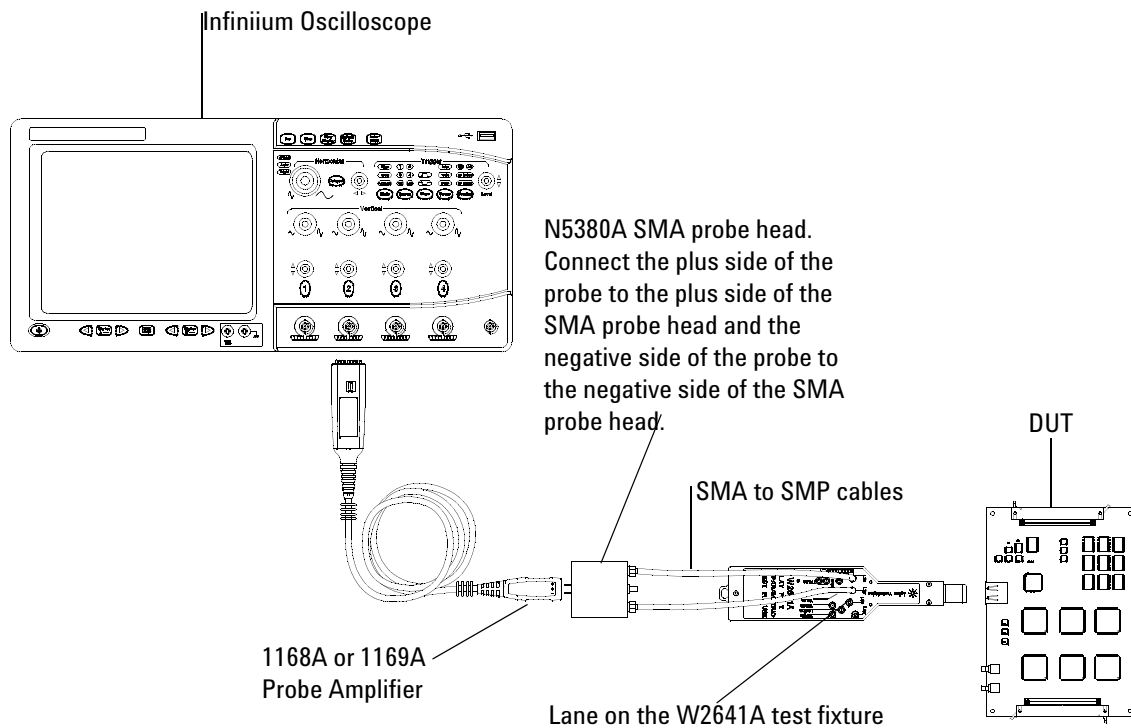


Figure 19 Probing for Differential Tests - Non Pre-Emphasis Level Tests (Single Connection with W2641A DisplayPort Test Fixture)

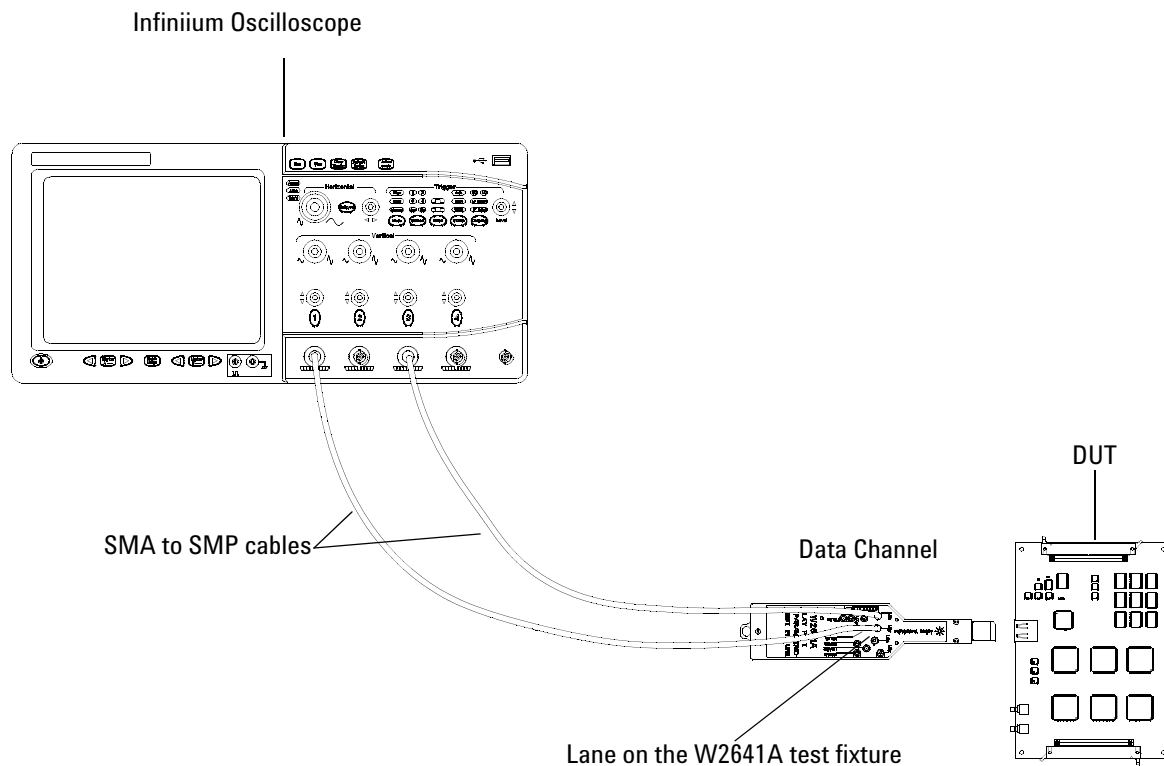


Figure 20 Differential Measurement Setup Using Two Single Ended Connections - Non Pre-Emphasis Level Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Non Pre-Emphasis Level Test

To evaluate the waveform peak differential amplitude to ensure signal is neither over, nor under driven. (Reference: Table 3.10 VESA DisplayPort Standard).

The source is given a range of expected output for each level setting that correlates with the system budget elements such as cable loss and receiver eye minimum and max values. This test ensures that the system budget is obeyed.

The amplitude measurement is performed using the following equation at all bit rates without pre-Emphasis and a PRBS 7 waveform:

$$\text{Peak-to-peak Voltage} = V_H - V_L$$

where:

V_H is the high voltage level

V_L is the low voltage level

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 Navigate to the Non-Pre-Emphasis Level - Lane # - Non Pre-Emphasis Level Test where # is the lane number to be tested.

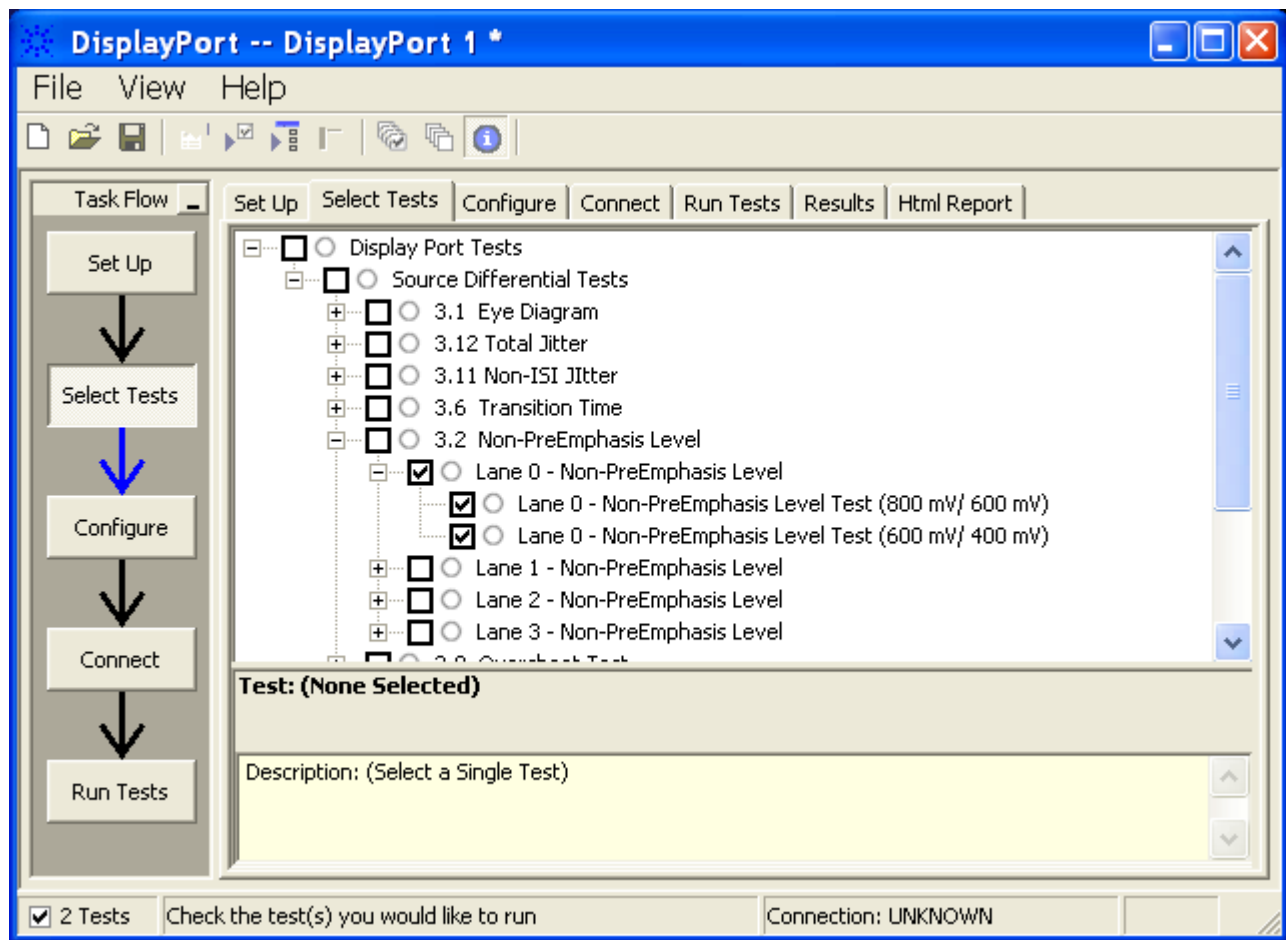


Figure 21 Selecting Non Pre-Emphasis Level Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 8](#)), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 8 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 8 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Non Pre-Emphasis	
Level Edges	Sets the number of edges measured for the level test.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

For each level setting testes, the following equation should be used:

$$\text{Resultant} = 20 * \log_{10}[\text{VoltagePeak-Peak\_Level A} / \text{VoltagePeak-Peak\_Level B}]$$

Table 9 Compared Levels

Measurement	Voltage _{Peak-Peak_LevelA}	Voltage _{Peak-Peak_LevelB}
1	600mV nominal (0 dB)	400mV nominal (0 dB)
2	800mV nominal (0 dB)	600mV nominal (0 dB)
3*	1200mV nominal (0 dB)*	800mV nominal (0 dB).
* if device optionally capable		

The resultants specifications are as identified below:

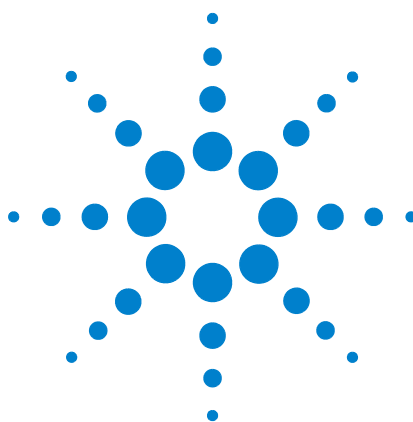
Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Test References

See Test 3-2: Non Pre-Emphasis Level Verification Testing, in the *DisplayPort-Compliance Test Specification Version 1.1*.



8 Source Overshoot Differential Tests (Informative)

Probing for Source Overshoot Differential Tests [70](#)

Source Overshoot Differential Tests [72](#)

This section provides the guidelines for source overshoot differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Overshoot Differential Tests

When performing the overshoot test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 22 and Figure 23 below show the differential and the single-ended connections for Overshoot Differential Tests.

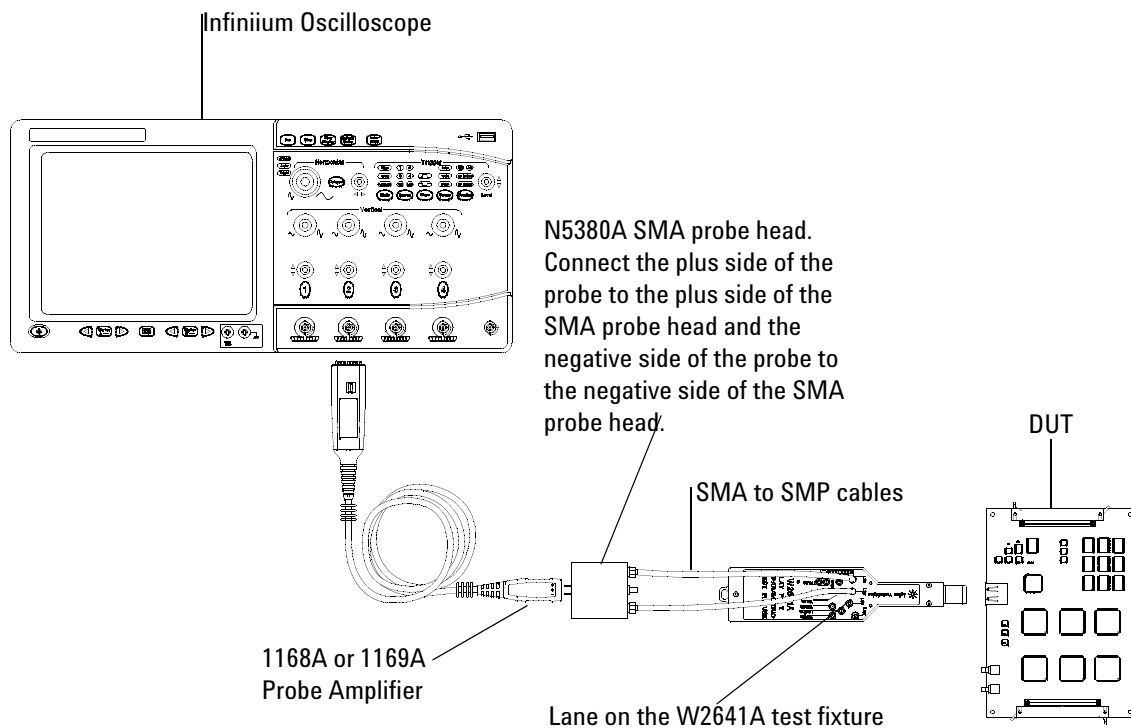


Figure 22 Probing for Differential Tests - Overshoot Tests (Single Connection with W2641A DisplayPort Test Fixture)

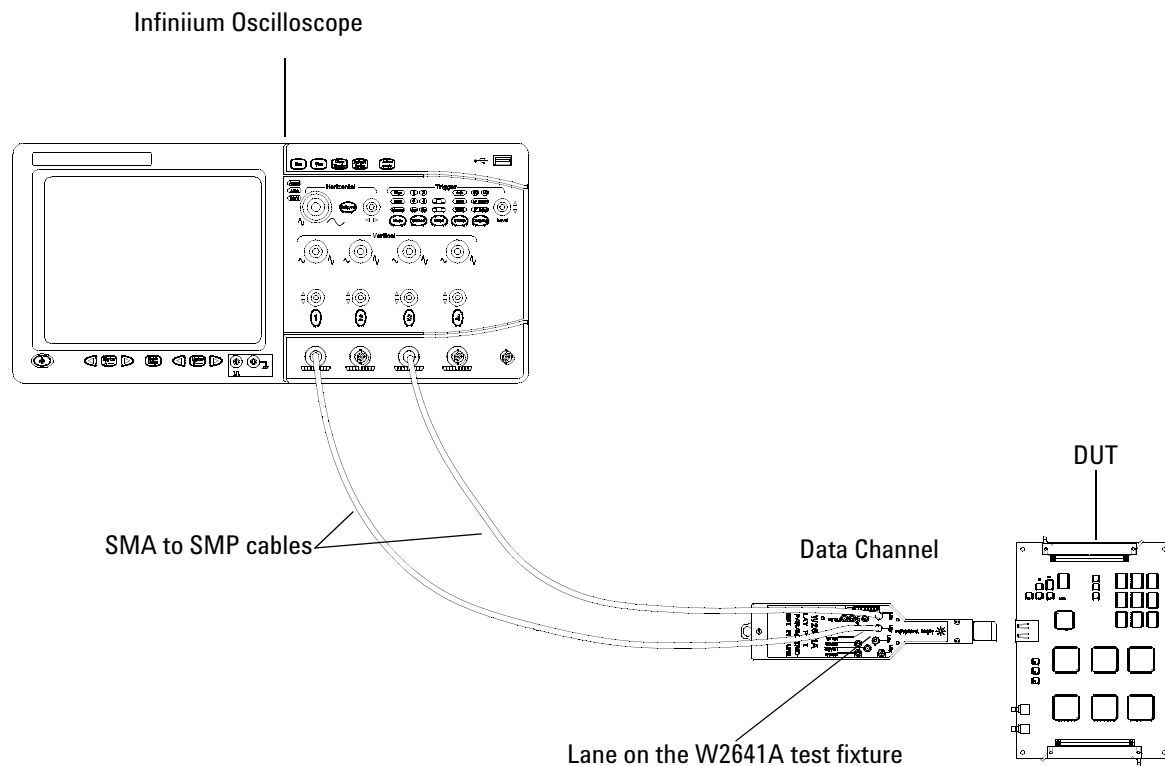


Figure 23 Differential Measurement Setup Using Two Single Ended Connections - Overshoot Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Overshoot Differential Tests

Overshoot is a differential measurement across the outputs of a differential pair. The overshoot test should be performed at the lowest pixel rate.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 This is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

Navigate to the Overshoot Test - Lane # - Overshoot Test where # is the lane number to be tested.

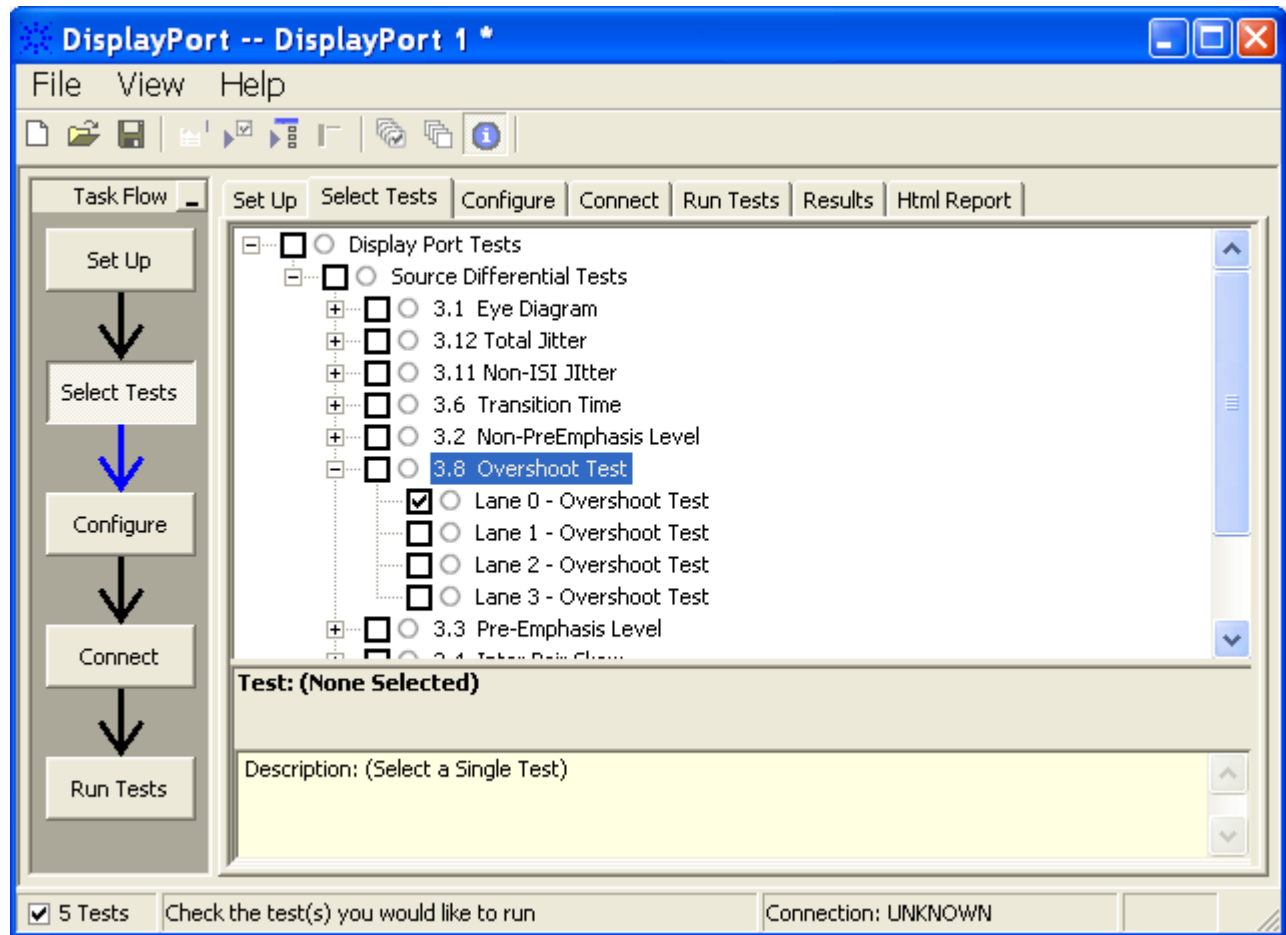


Figure 24 Selecting Overshoot Differential Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 10](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 10 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 10 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

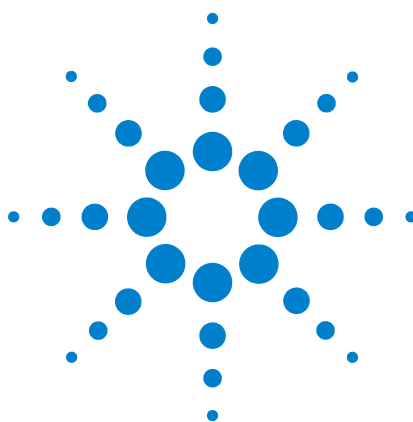
SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Overshoot $\leq$ 25% of the differential swing.

Test References

See section 3.8, in the *DisplayPort-Compliance Test Specification Version 1.1*.



9

Source Pre-Emphasis Level Differential Tests (Normative & Informative)

Probing for Source Pre-Emphasis Level Differential Tests 78

Source Pre-Emphasis Level Differential Tests 80

This section provides the guidelines for source pre-Emphasis level differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application. In this source test, the Pre-Emphasis Level tests are normative tests whereas Non-Transition Voltage Range Measurements are informative tests.



Probing for Source Pre-Emphasis Level Differential Tests

When performing the pre-Emphasis level differential test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 25 and Figure 26 below show the differential and the single-ended connections for Pre-Emphasis Level Differential Tests.

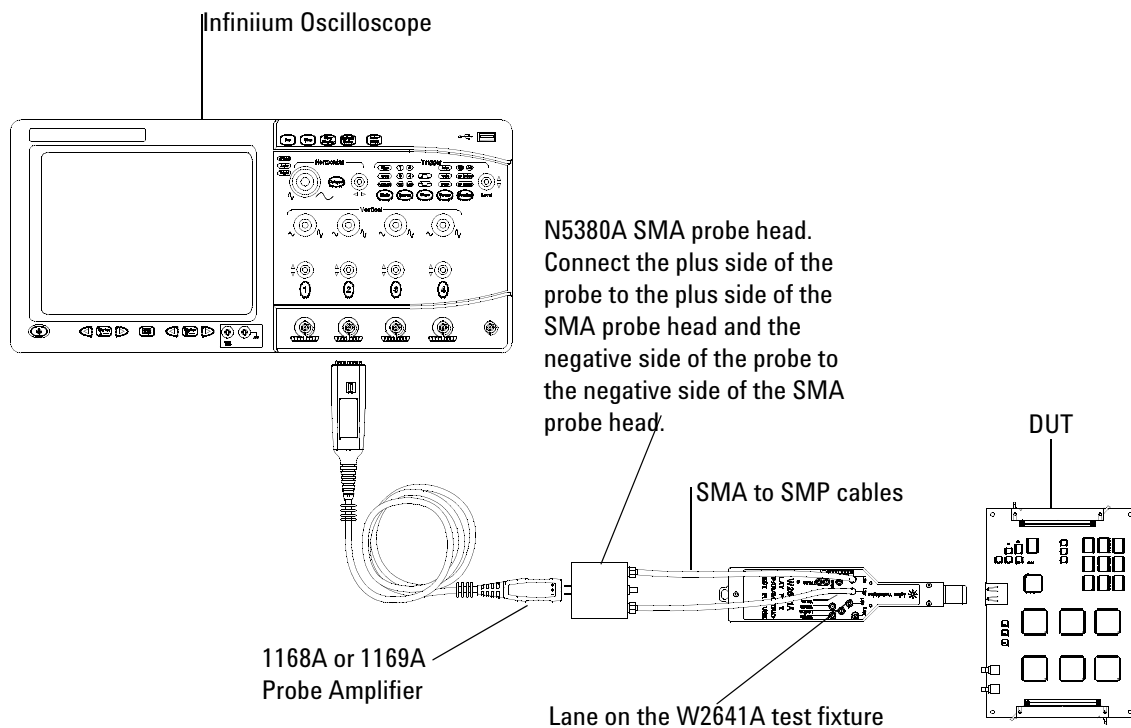


Figure 25 Probing for Differential Tests - Pre-Emphasis Level Tests (Single Connection with W2641A DisplayPort Test Fixture)

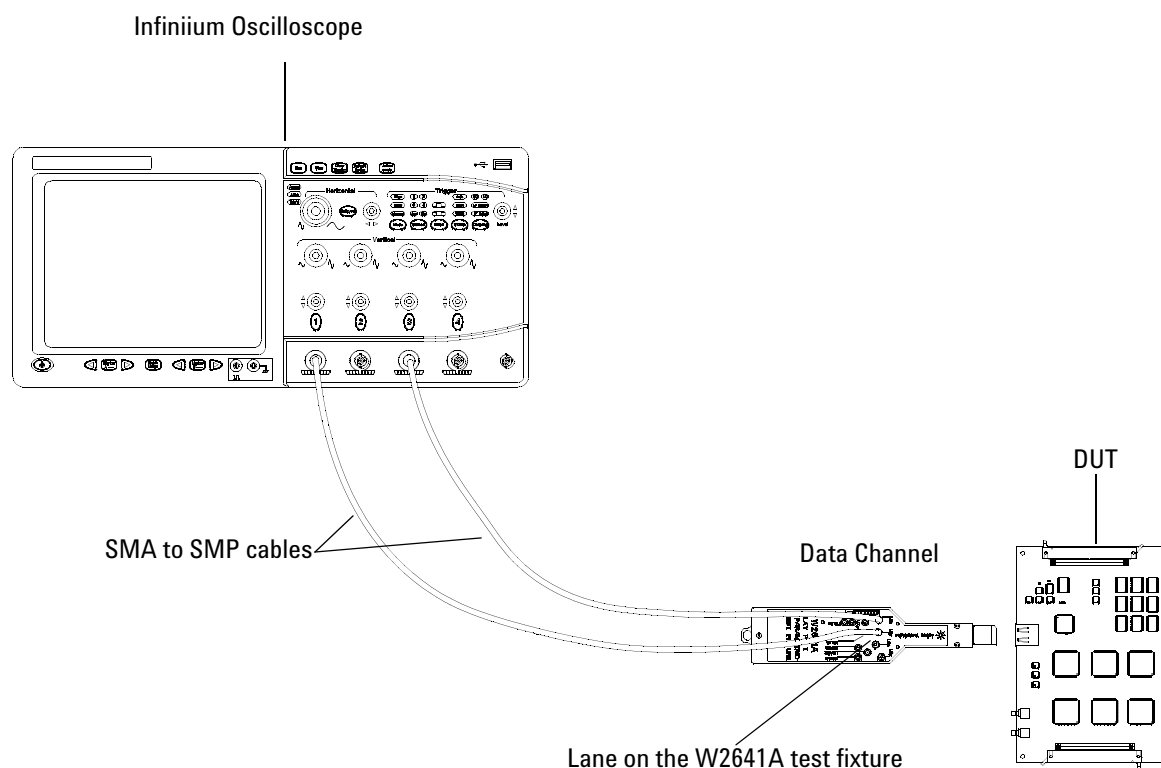


Figure 26 Differential Measurement Setup Using Two Single Ended Connections - Pre-Emphasis Level Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Pre-Emphasis Level Differential Tests

This test evaluates the effect of pre-Emphasis on the source waveform by measuring the peak differential amplitude and assuring the accuracy of the pre-Emphasis setting. (Reference: Table 3.10 VESA DisplayPort Standard).

The source can apply pre-Emphasis to the waveform in order to overcome the harmful effects caused by such things as system losses through pc boards, connectors, and cables. The standard stipulates the relative magnitude to overcome specific losses. Because pre-Emphasis is negotiated, two units with substantially different degrees of pre-Emphasis may be seen as non-interoperable under certain conditions. This test ensures that the system loss or pre-Emphasis budget is obeyed.

Tests must be made on all bit rates supported with pre-Emphasis for all differential voltage swings supported using a test pattern of PRBS 7. The following equation is used to calculate the pre-Emphasis result:

$$\text{Pre-emphasis Result} = 20 \log \left(\frac{V_{\text{Swingpe}}}{V_{\text{Swingnope}}} \right)$$

$$V_{\text{Swingpe}} = (V_{\text{Hpe}} - V_{\text{Lpe}})$$

$$V_{\text{Swingnope}} = (V_{\text{Hnope}} - V_{\text{Lnope}})$$

where:

V_{Hpe} = the high voltage value is measured using the histogram modes at the top for transition eyes.

V_{Lpe} = the low voltage value is measured using the histogram modes at the top for transition eyes.

V_{Hnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

V_{Lnope} = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels

of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.

- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 The Non-Transition Voltage Range Measurement test is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

9 Source Pre-Emphasis Level Differential Tests (Normative & Informative)

Navigate to the Pre-Emphasis Level - Lane # - Pre-Emphasis Level Test or Lane # - Non-Transition Voltage Range Measurement where # is the lane number to be tested.

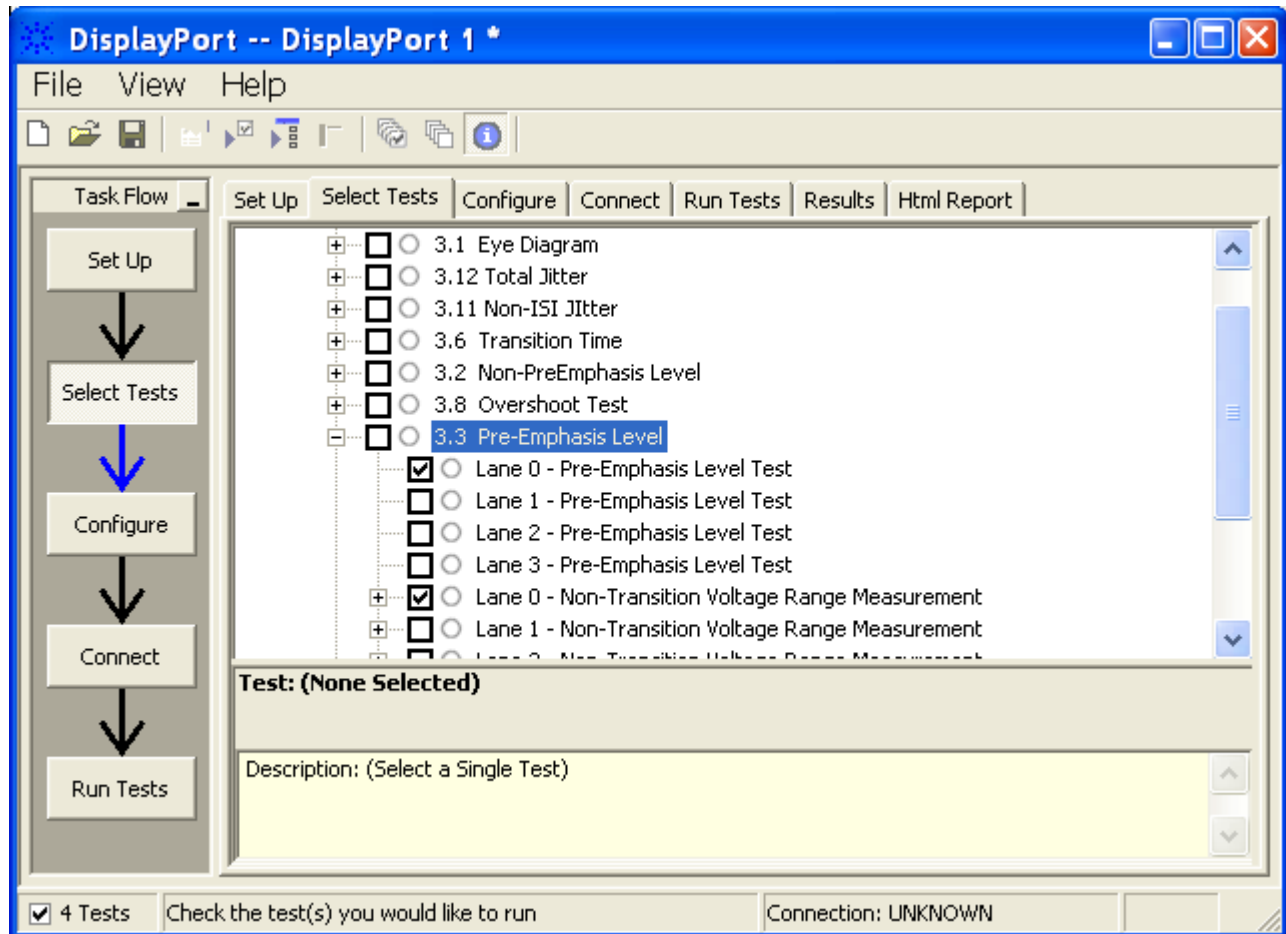


Figure 27 Selecting Pre-Emphasis Level Differential Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 11](#)), make oscilloscope connections, run the tests, and view the test results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 11 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.

Table 11 Test Configuration Options

Configuration Option	Description
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
PreEmphasis Level	
PreEmphasis Edge	Sets the number of edges measured for the Pre-Emphasis Level test.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: all the pre-Emphasis supported settings are subject to the constraints listed in Table 3-12 of the DisplayPort Standard.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

The pre-Emphasis calculation must fall within the following ranges for each pre-Emphasis level:

0 dB setting: Resultant ≥ -8.4 dB

3.5 dB setting: Resultant3.5dB ≥ 2.0 dB

6.0 dB setting: Resultant6.0dB $\geq$ Resultant3.5dB + 1.6

9.5 dB setting: Resultant9.5dB $\geq$ Resultant6.0dB + 1.6

The non-transition voltage range measurement calculation must fall within the following ranges:

Resultant $< 0.30 * (\text{Nominal Voltage})$

400 mV: Resultant $< 120\text{mV}$

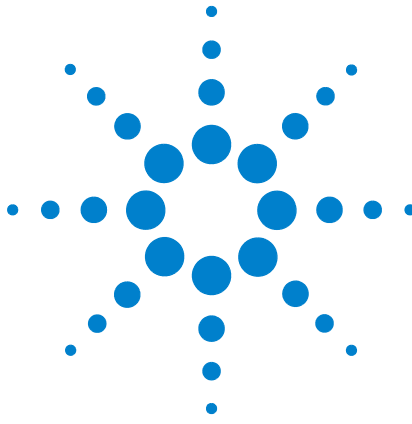
600 mV: Resultant $< 180\text{mV}$

800 mV: Resultant $< 240\text{mV}$

Test References

See Test 3-3: Pre-Emphasis Level Verification Testing, in the *DisplayPort-Compliance Test Specification Version 1.1*.

9 Source Pre-Emphasis Level Differential Tests (Normative & Informative)



10

Source Inter Pair Skew Differential Tests

Probing for Source Inter Pair Skew Differential Tests [88](#)

Source Inter Pair Skew Differential Test [90](#)

This section provides the guidelines for source inter pair skew differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Inter Pair Skew Differential Tests

When performing the inter pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 28 and Figure 29 below show the differential and the single-ended connections for Inter Pair Skew Differential Tests..

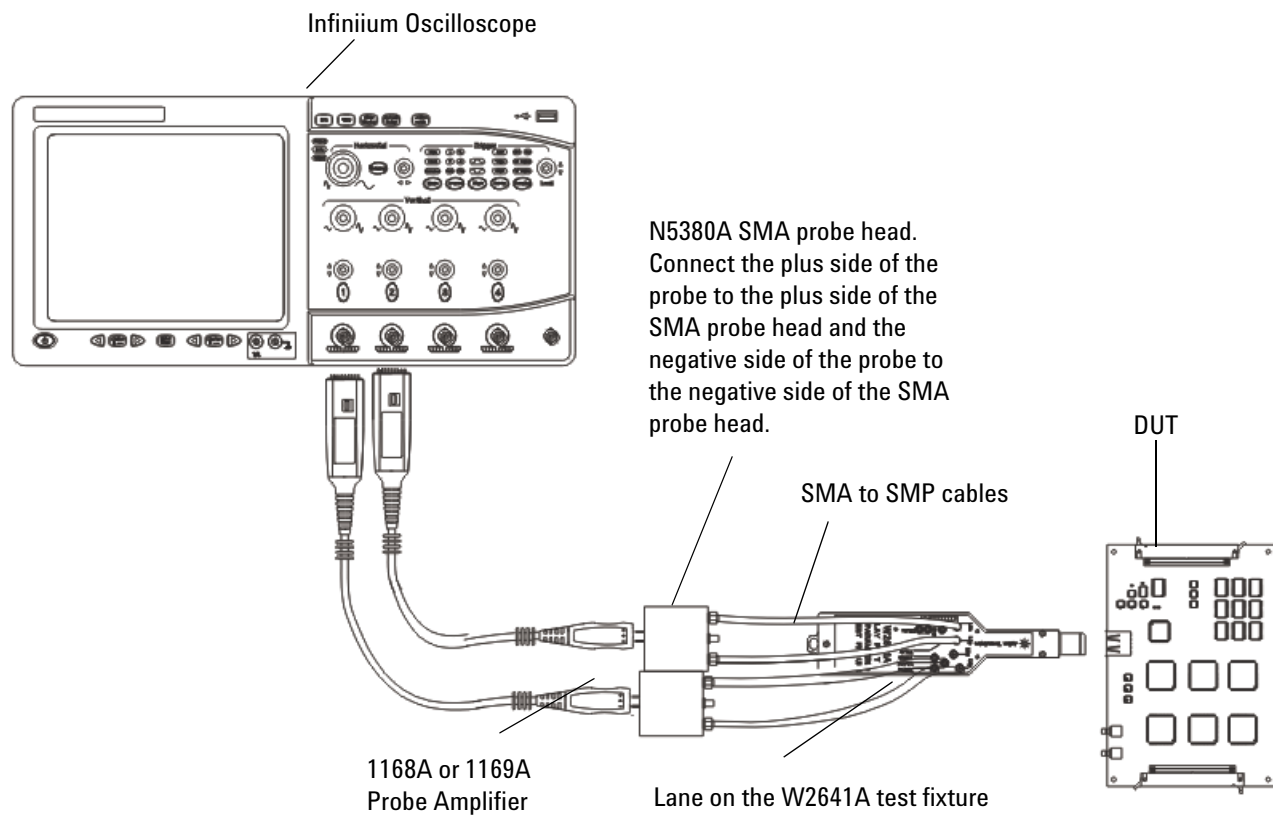


Figure 28 Probing for Differential Tests - Inter Pair Skew Tests (Single Connection with W2641A DisplayPort Test Fixture)

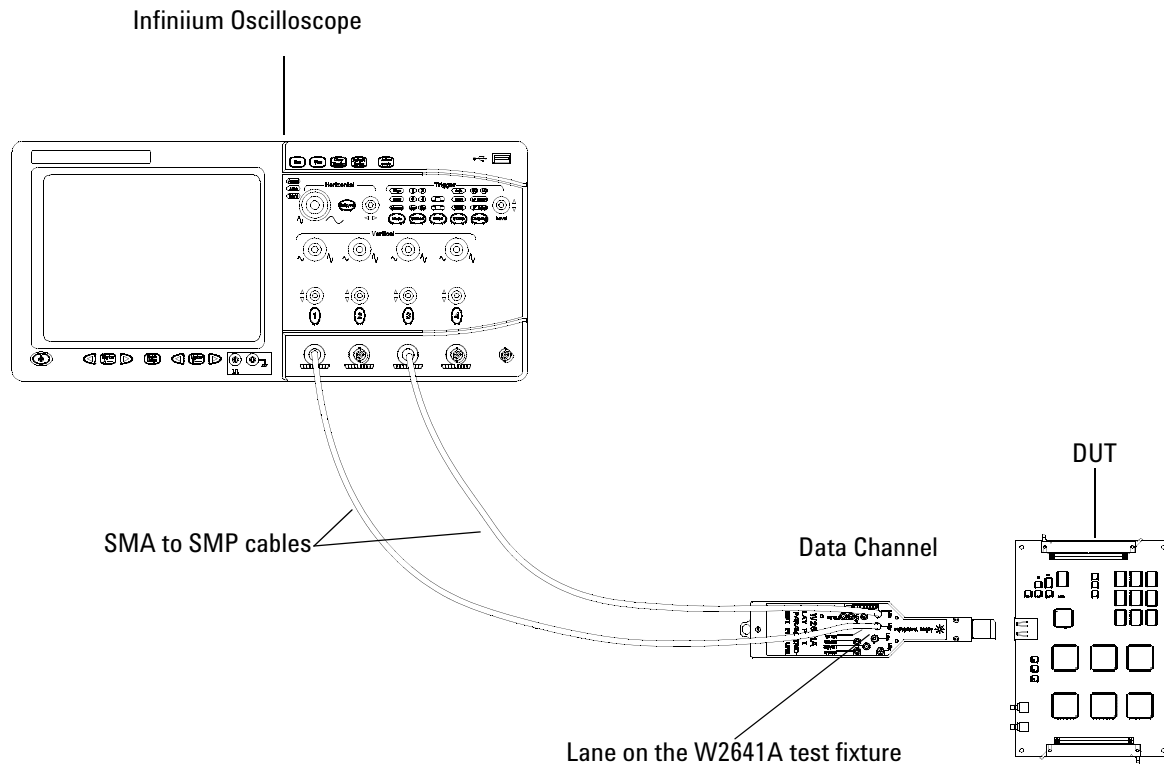


Figure 29 Differential Measurement Setup Using Two Single Ended Connections - Inter Pair Skew Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Inter Pair Skew Differential Test

The inter pair skew test evaluates the skew, or time delay, between respective differential data lanes in the DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard).

The DisplayPort interface has the ability to skew, or deskew lanes by 20 UI (Unit Intervals) which is as much as 12ns (1.62Gb/s) and is intended to eliminate simultaneous degradation of concurrent bytes of transmitted data. The specification at 150 ps at the package pins (TP1), likely to be degraded another 50 ps through the connector, is less than 0.5 UI at the highest bit rate. Therefore, it is unlikely to be a significant reason for non-interoperability.

Channel-to-channel de-skew must be performed on the two oscilloscope channels used for this measurement (see [“Differential Probe Head Skew Calibration”](#) on page 223 and [“SMA Probe Head Skew Calibration”](#) on page 229).

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the Inter Pair Skew - Lane # - Inter Pair Skew Test where # is the lane number to be tested.

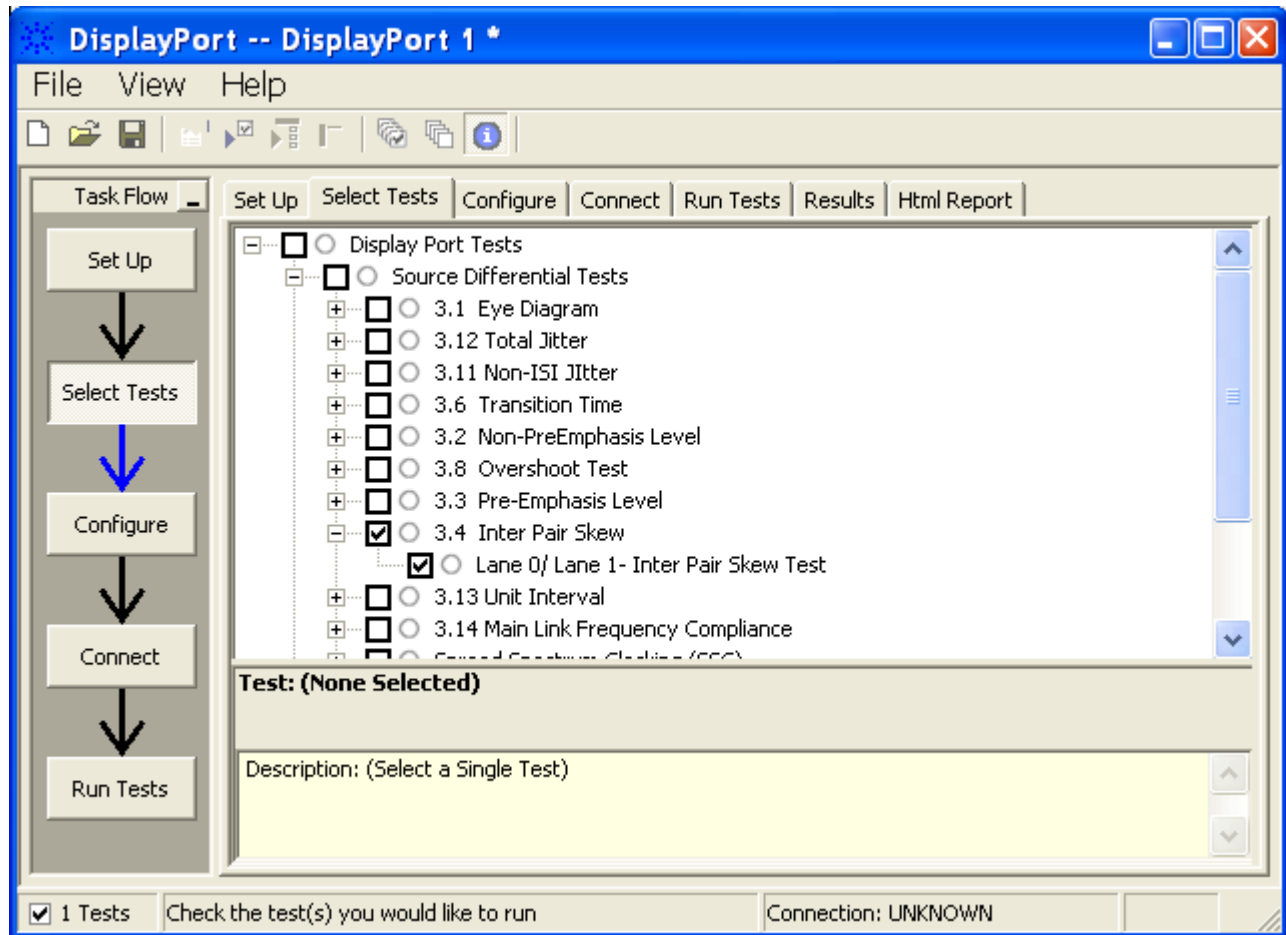


Figure 30 Selecting Inter Pair Skew Differential Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 12](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 12 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 12 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Source Differential Tests	
Inter Pair Skew	
Inter Pair Skew Edges	Sets the number of edges measured for the inter pair skew test.
Maximum Retries	Sets the number of re-tries for the inter pair skew test.
Trigger Patterns	Define trigger pattern other than the default pattern.

Test Condition

Bit Rate: highest bit rate is supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

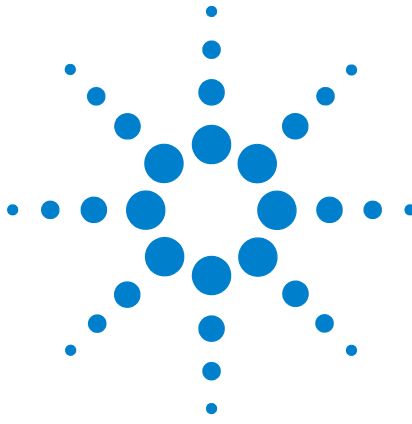
SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

$-2 \text{ UI} \leq \text{Inter Pair Skew} \leq 2 \text{ UI}$

Test References

See Test 3.4: Inter-Pair Skew Measurement, in the *DisplayPort-Compliance Test Specification Version 1.1*.



11

Source Unit Interval Differential Tests (Informative)

Probing for Source Unit Interval Differential Tests 96

Source Unit Interval Differential Tests 98

This section provides the guidelines for source unit interval differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Unit Interval Differential Tests

When performing the unit interval test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 31 and Figure 32 below show the differential and the single-ended connections for Unit Interval Differential Tests.

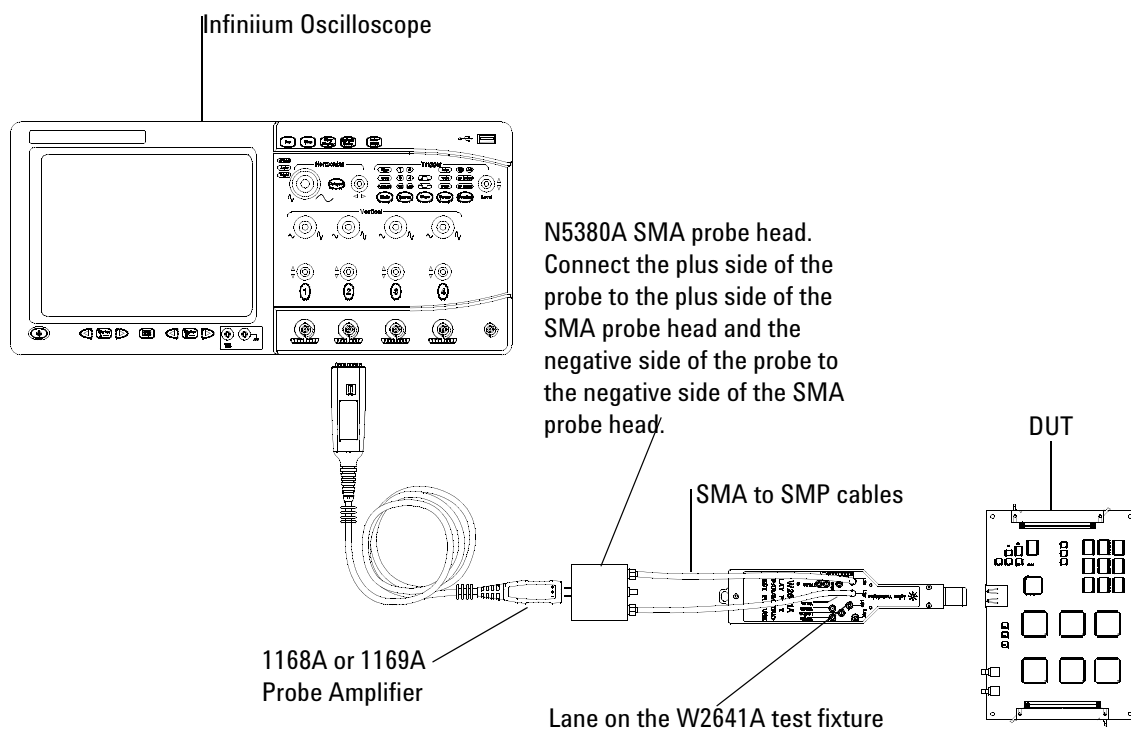


Figure 31 Probing for Differential Tests - Unit Interval Tests (Single Connection with W2641A DisplayPort Test Fixture)

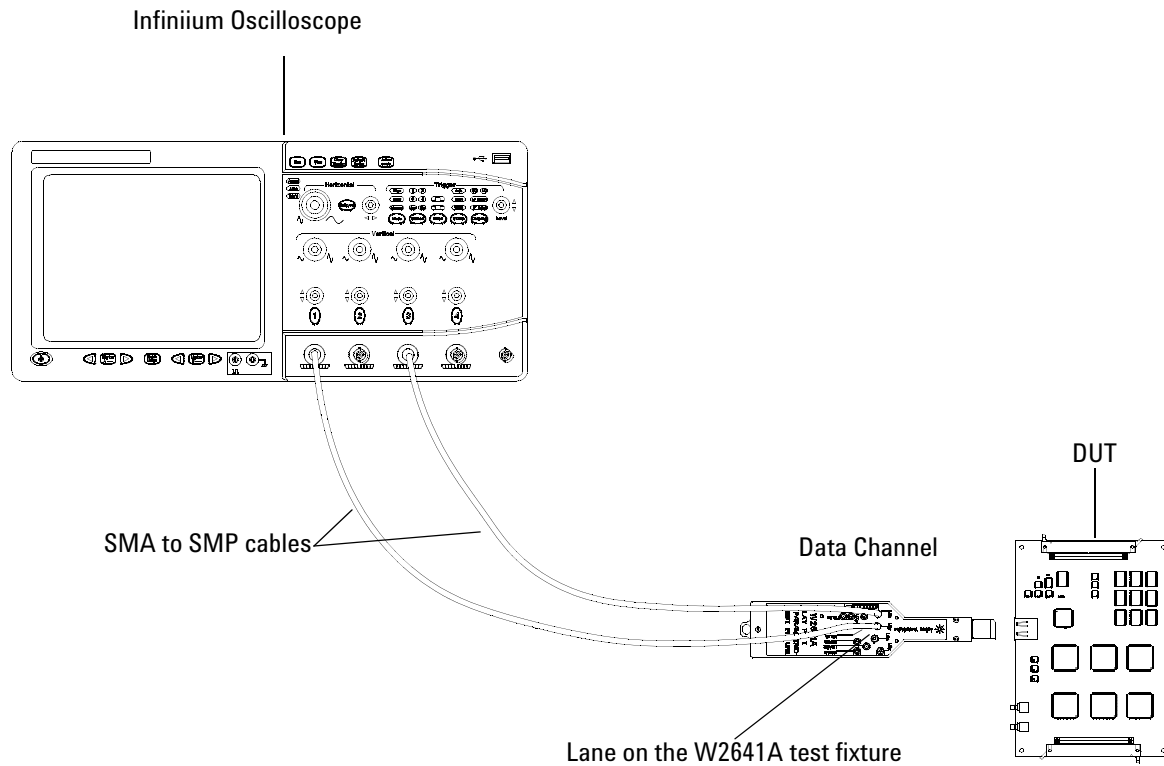


Figure 32 Differential Measurement Setup Using Two Single Ended Connections - Unit Interval Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Unit Interval Differential Tests

Unit interval test evaluates the overall variation in the UI width over at least one full typical SSC cycle to ensure it stays within the specification limit.

This test calculates the average unit interval with and without the spread spectrum clocking which will have very little to do with interoperability unless the unit interval is at the extremes.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 This is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

Navigate to the Unit Interval - Lane # - SSC Unit Interval Test where # is the lane number to be tested.

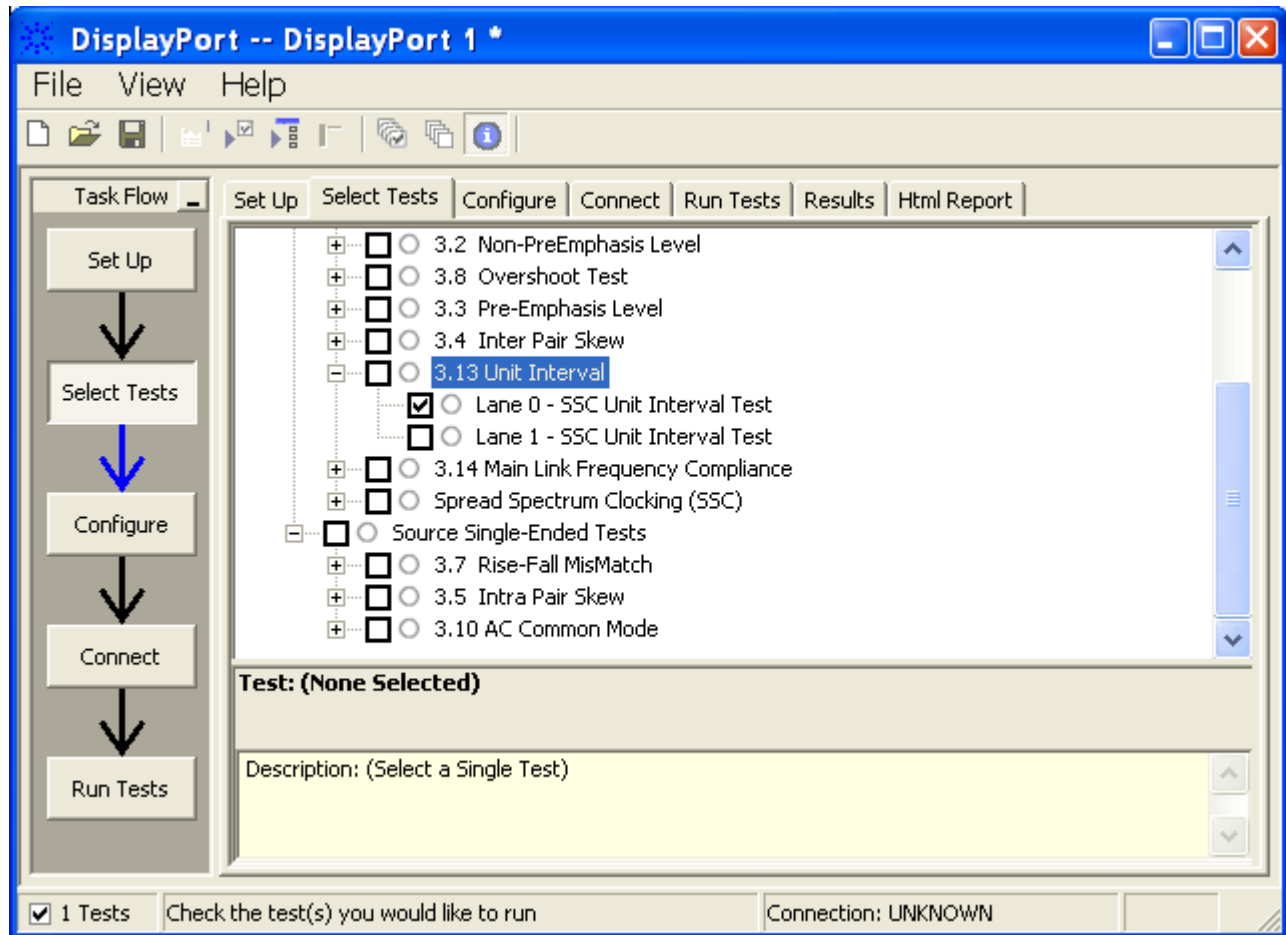


Figure 33 Selecting Unit Interval Differential Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 13](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

11 Source Unit Interval Differential Tests (Informative)

Table 13 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 13 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

An evaluation of at least 100K Unit Intervals or 1 full SSC cycle is required to ensure that any SSC modulation on the signal does not violate the timebase accuracy specifications.

PASS Condition

For Reduced Bit Rate:

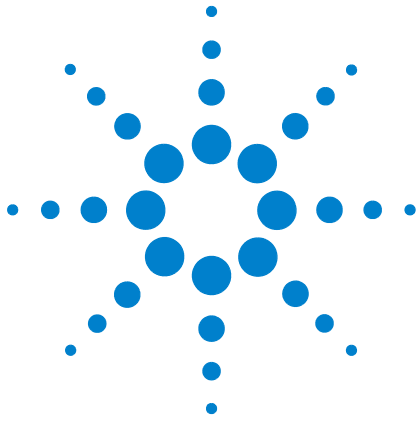
$$[1/1.62e9] * [1 - 0.0003] \leq \text{Mean Unit Interval} \leq [1/1.62e9] * [1 + 0.0053]$$

For High Bit Rate:

$$[1/2.7e9] * [1 - 0.0003] \leq \text{Mean Unit Interval} \leq [1/2.7e9] * [1 + 0.0053]$$

Test References

See section 3.6, in the *DisplayPort-Compliance Test Specification Version 1.1*.



12

Source Main Link Frequency Compliance Differential Tests

Probing for Source Main Link Frequency Compliance Differential Tests [104](#)

Source Main Link Frequency Compliance Differential Tests [106](#)

This section provides the guidelines for the source main link frequency compliance tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Main Link Frequency Compliance Differential Tests

When performing the source main link frequency compliance tests, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 34 and Figure 35 below show the differential and the single-ended connections for Main Link Frequency Compliance Tests.

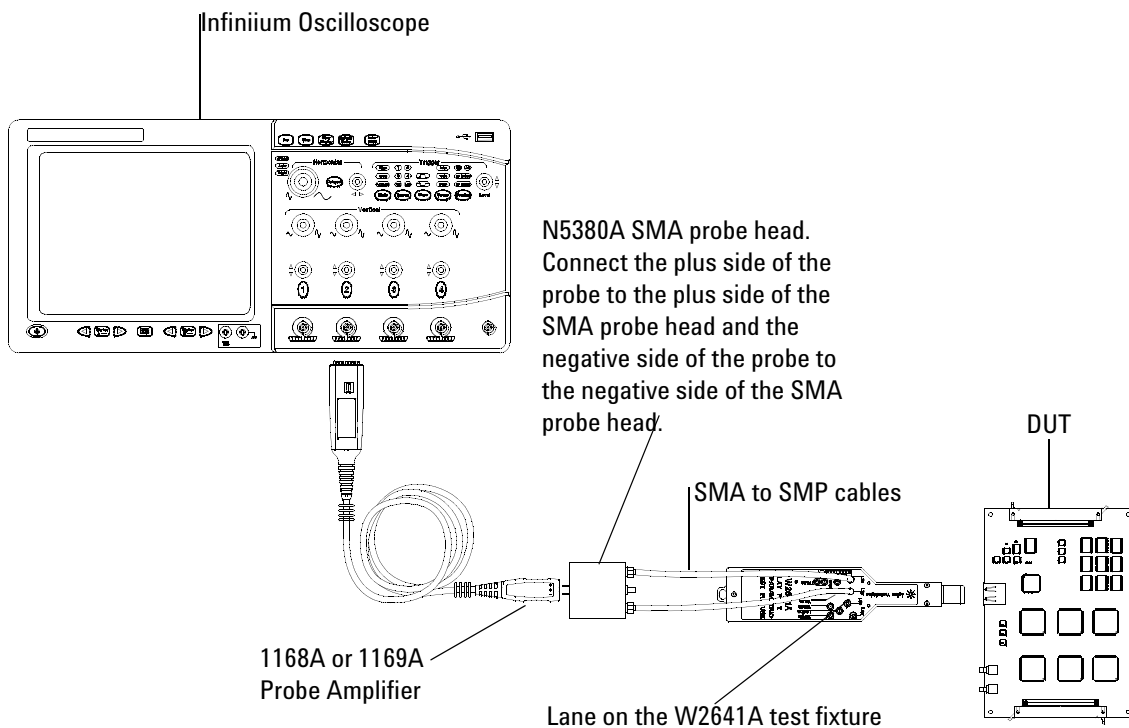


Figure 34 Probing for Differential Tests - Main Link Frequency Compliance Tests (Single Connection with W2641A DisplayPort Test Fixture)

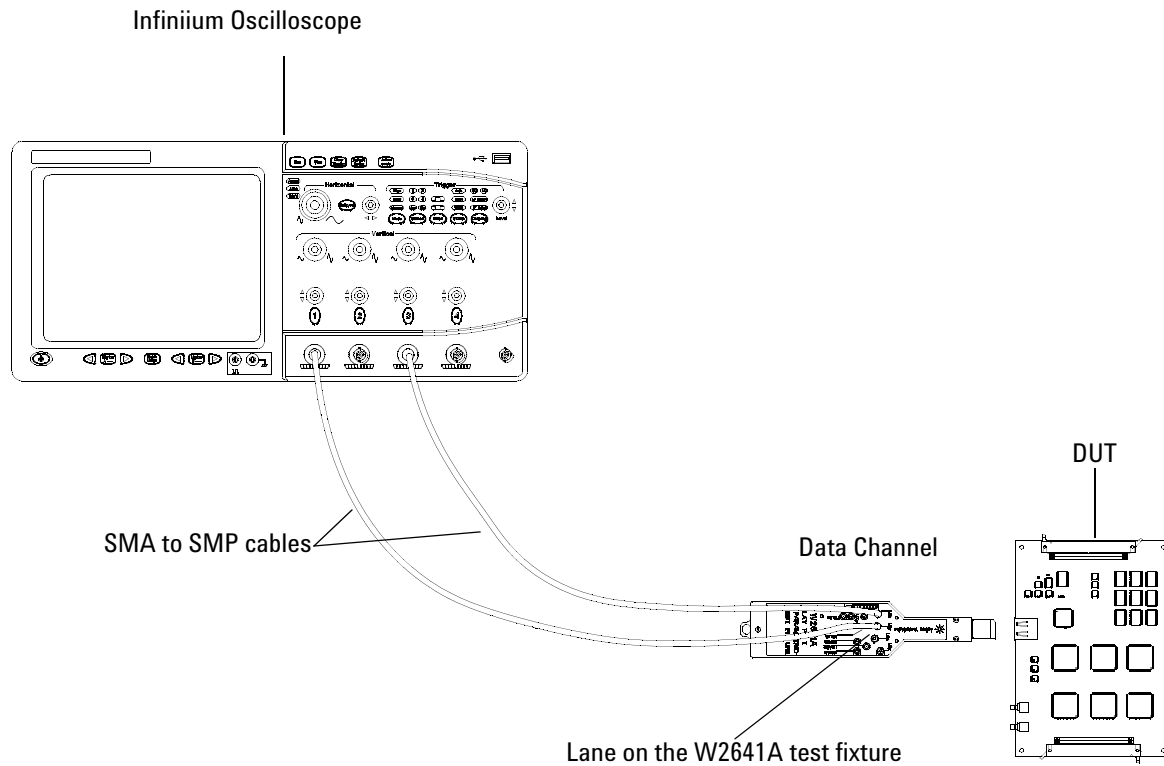


Figure 35 Differential Measurement Setup Using Two Single Ended Connections - Main Link Frequency Compliance Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Source Main Link Frequency Compliance Differential Tests

The main link frequency compliance test evaluates the overall variation in source time base accuracy, ensuring the device stays within the required ± 300 PPM limit. Tests shall be performed on a PRBS 7 signal with SSC disabled. An evaluation of at least 10 acquisitions is required.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the Main Link Frequency Compliance - Lane # - Main Link Frequency Compliance where # is the lane number to be tested.

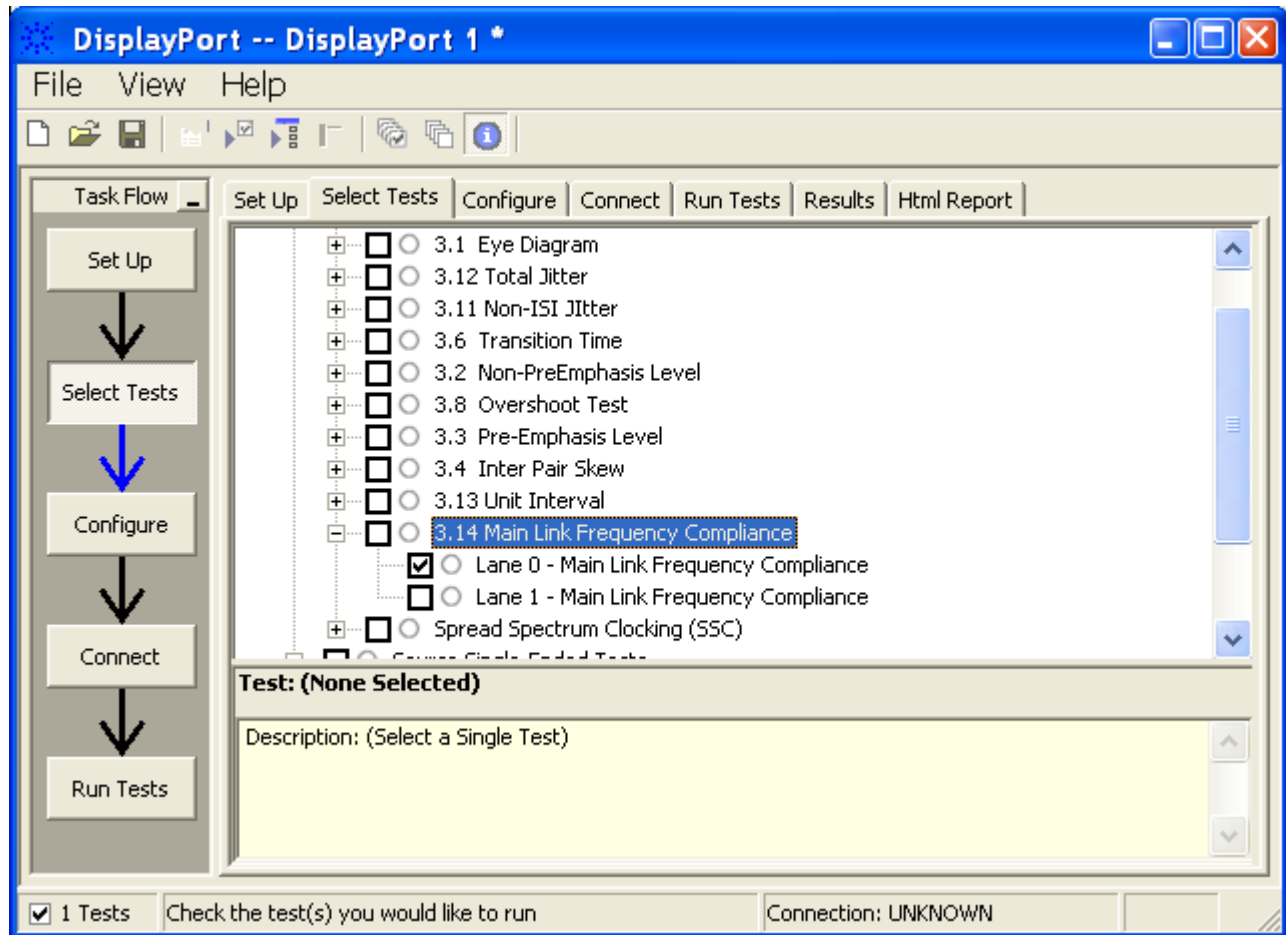


Figure 36 Selecting Main Link Frequency Compliance Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 14](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 14 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 14 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then the device is tested for both conditions. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

An evaluation of at least 10 full SSC cycles are required.

PASS Condition

The Main Link Frequency Compliance Test result must satisfy the following criteria:

SSC frequency_{ppm} ≤ 300.

Test References

See Test 3.14: Main Link Frequency Compliance Tests, in the *DisplayPort-Compliance Test Specification Version 1.1*.

12 Source Main Link Frequency Compliance Differential Tests



13 Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)

Probing for Source Spread Spectrum Clocking (SSC) Differential
Tests [112](#)

Source Spread Spectrum Clocking (SSC) Differential Test [114](#)

This section provides the guidelines for the source spread spectrum clocking (SSC) differential tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application. In this SSC test, the Modulation Frequency and Modulation Deviation tests are normative tests whereas Deviation HF Variation tests are informative tests.



Probing for Source Spread Spectrum Clocking (SSC) Differential Tests

When performing the spread spectrum clocking (SSC) test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 37 and Figure 38 below show the differential and the single-ended connections for Spread Spectrum Clocking (SSC) Differential Tests.

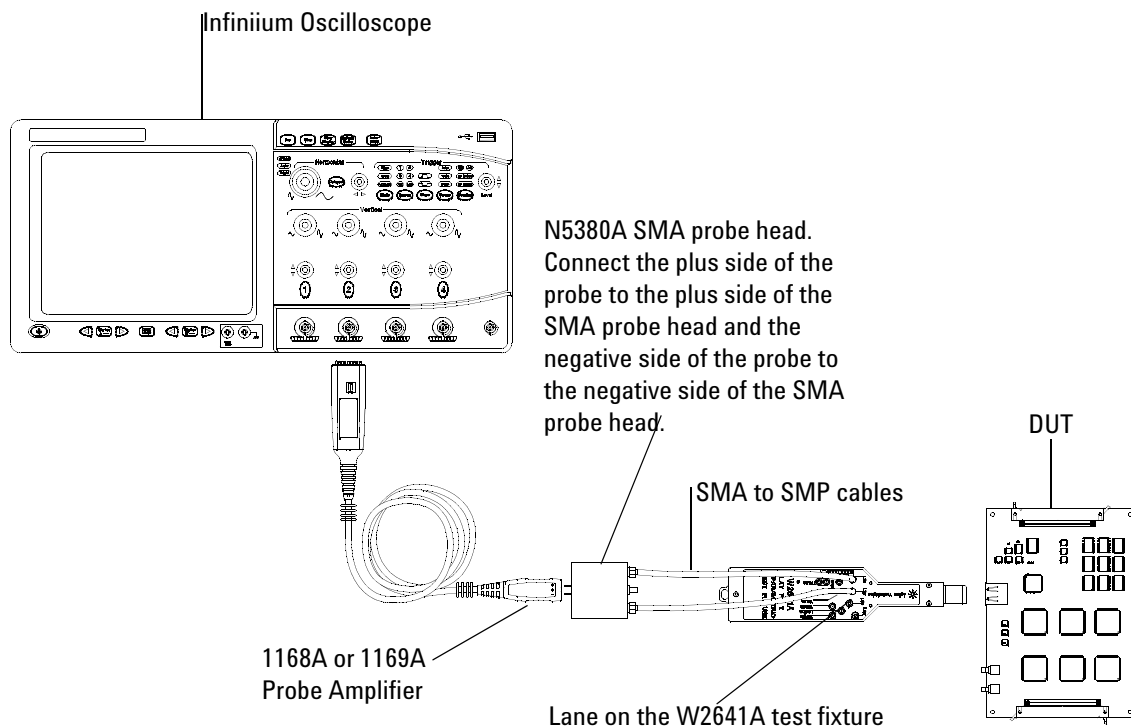


Figure 37 Probing for Differential Tests - SSC Tests (Single Connection with W2641A DisplayPort Test Fixture)

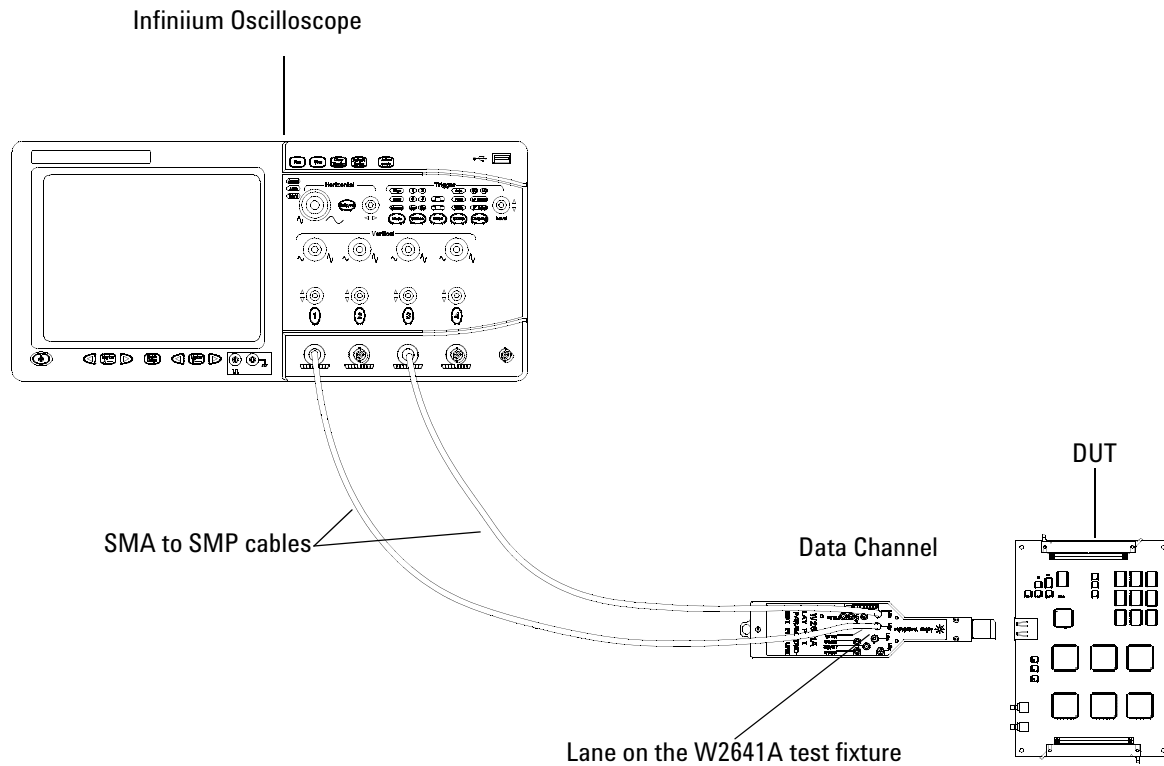


Figure 38 Differential Measurement Setup Using Two Single Ended Connections - SSC Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see [Chapter 25](#), “InfiniMax Probing,” starting on page 231.

Source Spread Spectrum Clocking (SSC) Differential Test

Spread Spectrum Modulation Frequency (Normative)

The spread spectrum modulation frequency evaluates the frequency of the SSC modulation and validates if it falls with specification limits.

The SSC frequency will be evaluated at the highest bit rate the transmitter supports. Tests shall be performed on a PRBS 7 signal, with SSC enabled. An evaluation of at least 10 full SSC cycles is required (Mean value reported). As SSC is mandatory, the reported result must be the mean of ten measured with maximum values from the range of SSC modulation deviation.

Spread Spectrum Modulation Deviation (Normative)

The spread spectrum modulation deviation evaluates the range of SSC down-spreading of the transmitter signal in PPM. This requires the device [the device must] operate in the region of 0 to -5000 PPM. The SSC Modulation Deviation will be evaluated at the highest bit rate the transmitter supports. Tests shall be performed on a PRBS 7 signal, with SSC enabled.

An evaluation of at least 10 full SSC cycles is required (Mean value reported). As SSC is mandatory, the reported result must be the mean of ten measured with maximum values from the range of SSC modulation deviation.

The value reported as the result must be the single total range value relative to nominal of the SSC modulation deviation, using the equation below, where "Min" is the mean of 10 recorded values of the minimum peaks.

Calculate deviation = (Measured Min - Nominal)/Nominal * 1e6 ppm

Deviation HF Variation (Informative)

The deviation HF variation verifies SSC profile that does not include any frequency deviations which would exceed 1250 ppm/μSec.

Spread spectrum clocking demands that the sink receiver tracks the modulated frequency of the source link rate while maintaining clock/data phase tracking. This test measures the range of frequency deviation with the source SSC enabled. If this range exceeds specification, the ability of the sink to frequency and phase track may be impaired, possibly causing data recovery errors and non-interoperability with a compliant receiver.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. SSC tests are available in the 2 test modes only- User Defined Conditions and Targeted Characterization Testing.
- 8 The Deviation HF Variation test is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked for this test.

13 Source Spread Spectrum Clocking (SSC) Differential Tests (Normative & Informative)

Navigate to the Spread Spectrum Clocking (SSC) group and select the appropriate test and the lane number to be tested.

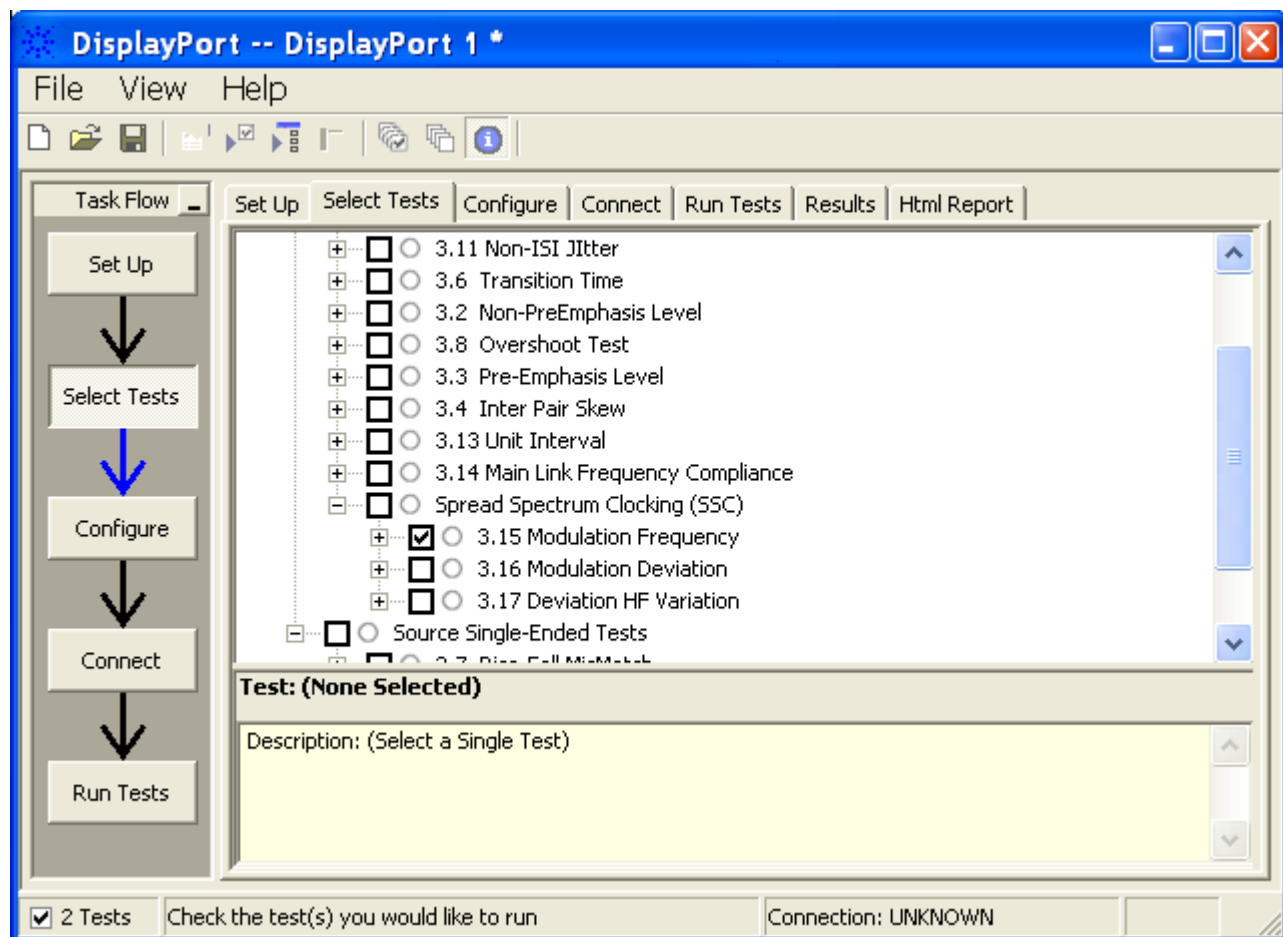


Figure 39 Selecting the Spread Spectrum Clocking (SSC) Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 15](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 15 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.

Table 15 Test Configuration Options

Configuration Option	Description
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

SSC Modulation Frequency Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Modulation Deviation Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Deviation HF Variation Test Condition

Bit Rate: highest rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: D10.2.

SSC: Enabled. The devices that do not have SSC Enabled will not be tested.

An evaluation of at least 10 full SSC cycle is required.

SSC Modulation Frequency PASS Condition

The SSC Modulation Frequency result must satisfy the following criteria:

- f_{SSC} measures between 30 kHz and 33 kHz

The value above shall be based on a mean of at least 10 complete SSC cycles.

SSC Modulation Deviation PASS Condition

The SSC Modulation Deviation result must satisfy the following criteria:

- SSC_{tol} measures between 5000 ppm and 0 ppm

The value above shall be based on a mean of at least 10 complete SSC cycles.

SSC Deviation HF Variation PASS Condition

The SSC Deviation HF Variation result must satisfy the following criteria:

- $SSC_t \text{ dF/dt} \leq 1250 \text{ ppm/}\mu\text{Sec}$ variations

The value above shall be based on a mean of at least 10 complete SSC cycles.

Test References

See Test 3.15: Spread Spectrum Modulation Frequency, Test 3.16: Spread Spectrum Modulation Deviation and Test 3.17: Deviation HF Variation in the *DisplayPort-Compliance Test Specification Version 1.1*.



14 Source Rise-Fall Mismatch Single-Ended Tests (Informative)

Probing for Source Rise-Fall Mismatch Single-Ended Tests [122](#)

Source Rise-Fall Mismatch Single-Ended Tests [123](#)

This section provides the guidelines for source rise-fall mismatch single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Rise-Fall Mismatch Single-Ended Tests

When performing the rise-fall mismatch test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 40 below shows the single-ended connections for the Rise-Fall Mismatch Single-Ended Tests.

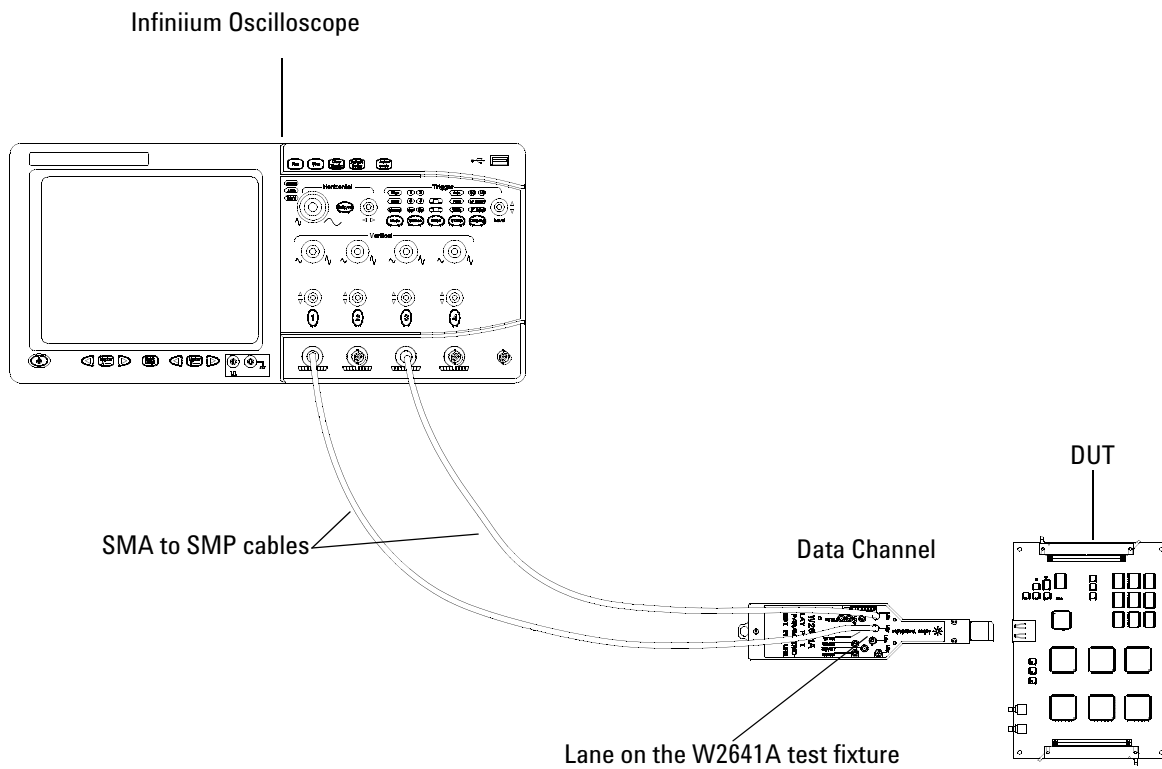


Figure 40 Differential Measurement Setup Using Two Single Ended Connections - Rise-Fall Mismatch Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source Rise-Fall Mismatch Single-Ended Tests

The rise and fall time mismatch tests evaluate the differences in rise and fall times of the two single-ended waveform in a given differential data lane of a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard specification).

The mismatch in time of the rising and falling time of the single-ended signals composing a differential lane will create common mode noise and will radiate.

The rise and fall times are measured between the 80% and 20% levels of the waveform.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.
- 8 This is an Informative test, therefore, the Hide Informative Tests checkbox must be un-checked.

14 Source Rise-Fall Mismatch Single-Ended Tests (Informative)

Navigate to the Rise-Fall Mismatch group, and check the Rising Mismatch or Falling Mismatch tests that you want to perform and the lane number to be tested.

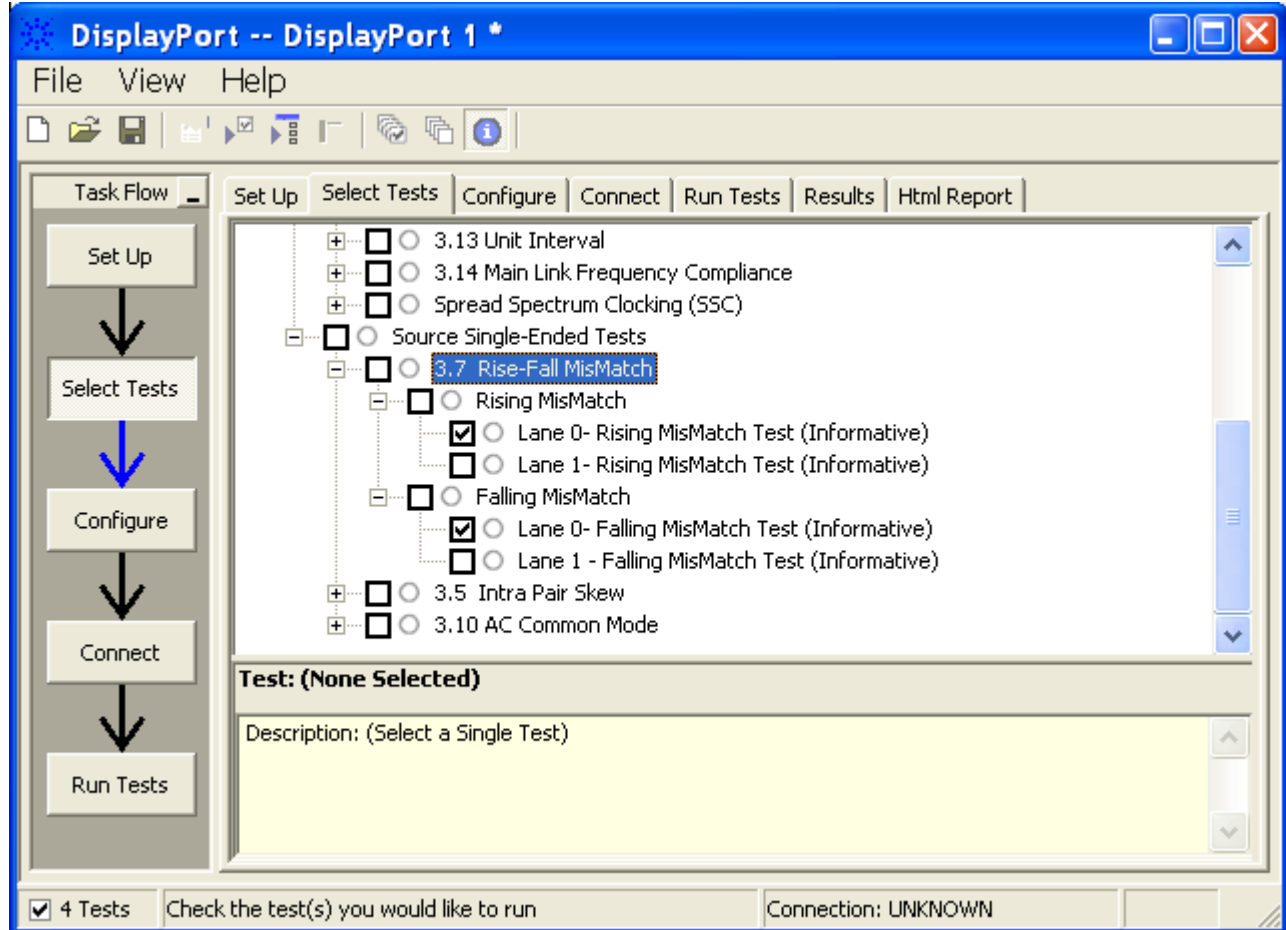


Figure 41 Selecting Rise-Fall Mismatch Tests

- 9 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 16](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 16 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 16 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Single-ended Tests	
Rise-Fall Mismatch	
Rise-Fall Mismatch Edge	Sets the number of edges measured for the rise-fall mismatch test.
Threshold	Sets the threshold used to make a rise time or fall time measurement.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then SSC Disabled will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

Two single-ended signals are probed independently, acquired simultaneously and compared.

PASS Condition

Falling Mismatch $\leq$ 15% of the single-ended rise time

Rising Mismatch $\geq$ 15% of the single-ended fall time

Test References

See section 3.7, in the *DisplayPort-Compliance Test Specification Version 1.1*.

14 Source Rise-Fall Mismatch Single-Ended Tests (Informative)



15 Source Intra Pair Skew Single-Ended Tests

Probing for Source Intra Pair Skew Single-Ended Tests [130](#)

Source Intra Pair Skew Single-Ended Tests [131](#)

This section provides the guidelines for source intra pair skew single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source Intra Pair Skew Single-Ended Tests

When performing the intra pair skew test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 42 below shows the single-ended connections for Intra Pair Skew Single-Ended Tests.

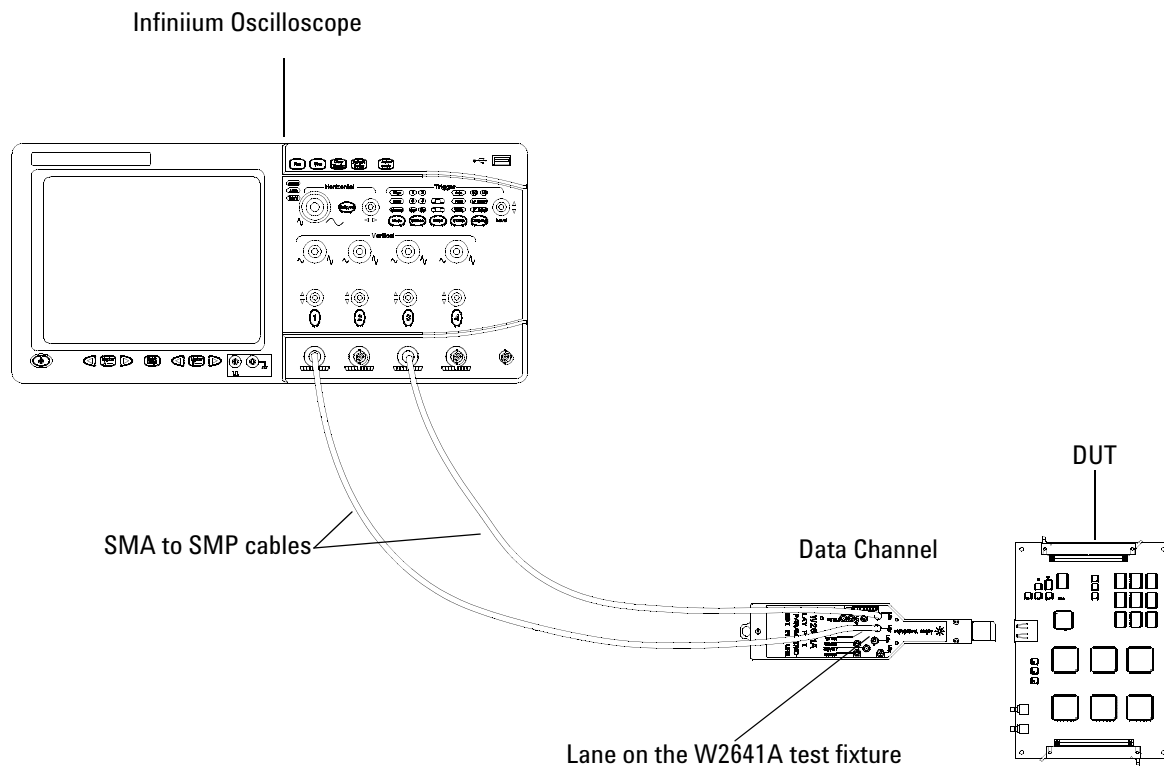


Figure 42 Differential Measurement Setup Using Two Single Ended Connections - Intra Pair Skew Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source Intra Pair Skew Single-Ended Tests

The intra pair skew test evaluates the skew, or time delay, between the respective sides of a differential data lane in a DisplayPort interface. (Reference Table 3.10 VESA DisplayPort Standard).

Intra pair skew has deleterious effects on signal rise time and manner of crossing through the transition point. The DisplayPort specification at package pins (TP1) is 20 ps. It can clearly double or triple to and through the connector. These are secondary contributors to source jitter performance.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

15 Source Intra Pair Skew Single-Ended Tests

Navigate to the Intra Pair Skew - Lane # - Intra Pair Skew Test where # is the lane number to be tested.

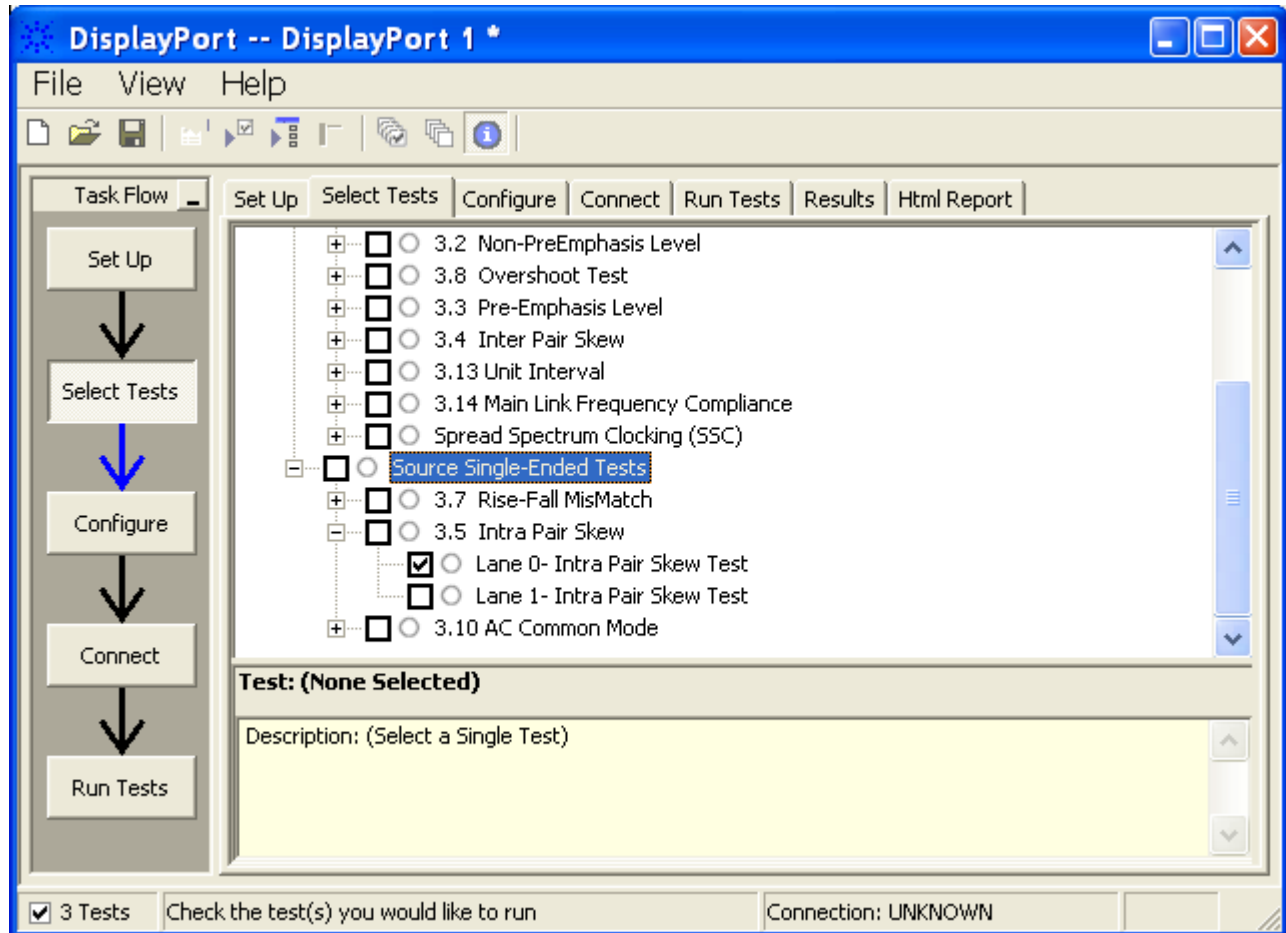


Figure 43 Selecting Intra Pair Skew Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 17](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 17 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 17 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Single-ended Tests	
Intra-pair Skew	
Intra Pair Skew Edges	Sets the number of edges measured for the intra pair skew test.
Skew Trigger Patterns	Define trigger pattern for intra pair skew test.

Test Condition

Bit Rate: highest bit rates are supported.

Output Level: 800 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

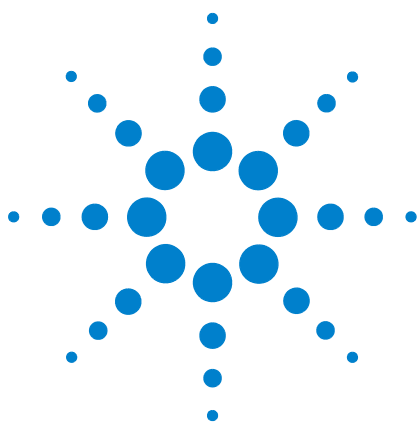
SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then both will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

PASS Condition

Intra pair skew $\leq$ 30 ps

Test References

See Test 3.5: in the *DisplayPort-Compliance Test Specification Version 1.1*.



16 Source AC Common Mode Noise Single-Ended Tests

Probing for Source AC Common Mode Noise Single-Ended Tests [138](#)
Source AC Common Mode Noise Single-Ended Test [139](#)

This section provides the guidelines for source AC common mode noise single-ended tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Source AC Common Mode Noise Single-Ended Tests

When performing the AC common mode noise test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 44 below shows the single-ended connections for AC Common Mode Noise Single-Ended Tests.

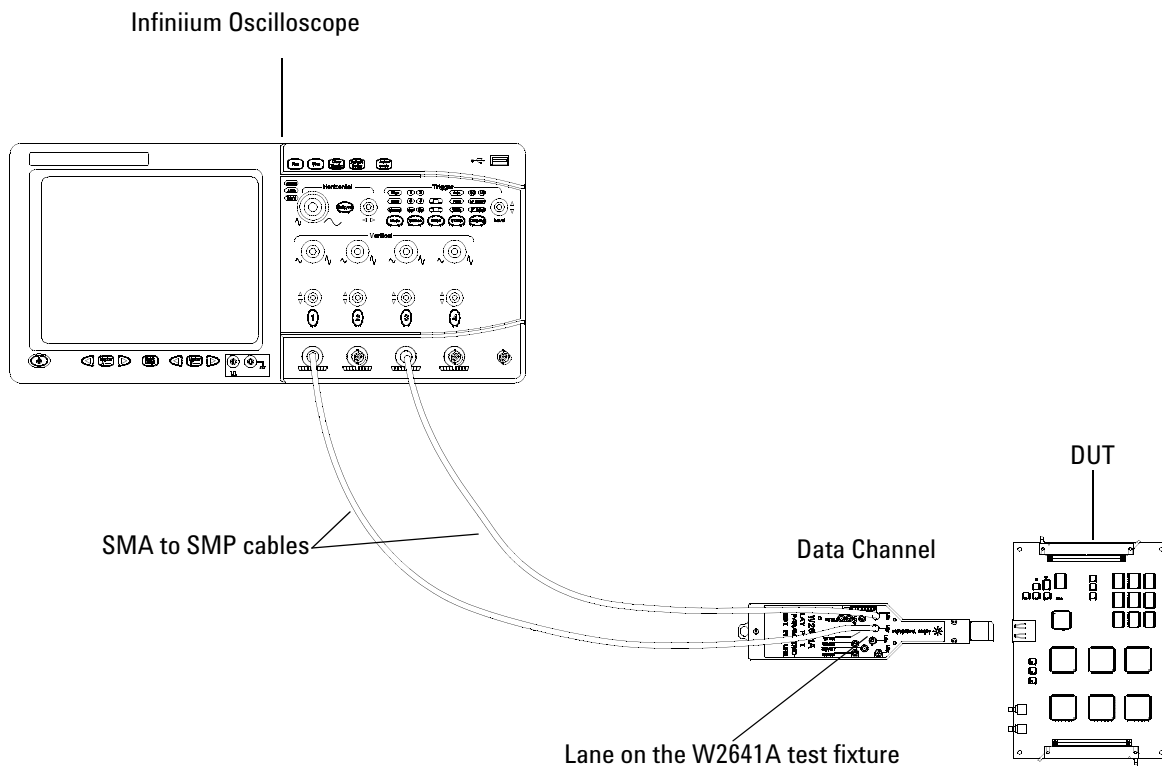


Figure 44 Differential Measurement Setup Using Two Single Ended Connections - AC Common Mode Noise Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Source AC Common Mode Noise Single-Ended Test

The AC common mode noise measurement of the distributed clock network verifies that the nominal operating clock frequency is within the acceptable tolerance range. In order for the sink devices to properly recover the data, the source clock must operate within the acceptable tolerance range.

The test must be made at all bit rates supported by the device under test without pre-Emphasis and a voltage swing of 1.2 volts. A test pattern of D10.2 should be used.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the Test Mode, Test Type, DUT Definition Settings, Fixture Type, Connection Type and Number of Channels according to the type of testing being done. Source tests are available in all the 3 test modes - Compliance Conditions Only, User Defined Conditions and Targeted Characterization Testing.

Navigate to the AC Common Mode - Lane # - Common Mode AC Test where # is the lane number to be tested.

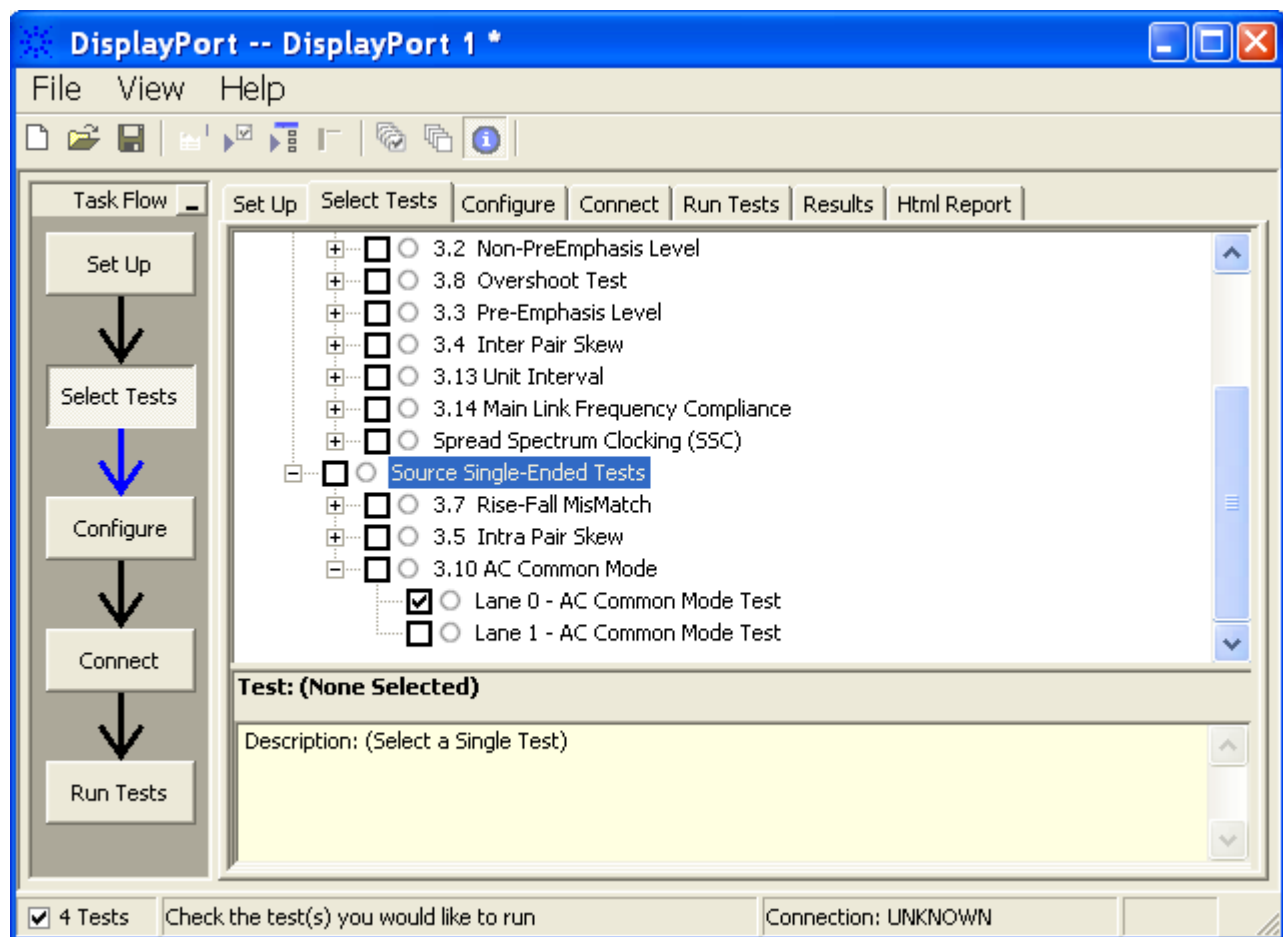


Figure 45 Selecting AC Common Mode Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 18](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 18 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 18 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.
Single-ended Tests	
AC Common Mode	
AC Common Edge	Sets the number of edges measured for the AC common mode test.
Interpolation	Specifies whether to turn on or off the Sin(x)/x interpolation. Turning On interpolation may cause more peak-to-peak jitter.
Filter	Specifies whether a high pass filter, low pass filter or no filter is applied before the measurement. Interpolation is turned off if any filter is chosen.
Cut Off Frequency	Sets the Cut Off Frequency if a Filter is applied.Specify in correct format; xMHz, xkHz or xHz.

Test Condition

Bit Rate: all bit rates are supported.

Output Level: all output levels are supported.

Pre-Emphasis: all the pre-Emphasis settings are supported.

Test Pattern: PRBS 7.

SSC: If the device under test is able to operate either with SSC Enabled or SSC Disabled then SSC Disabled will be selected. If the device is always SSC Enabled or always SSC Disabled then the device is tested in its normal state.

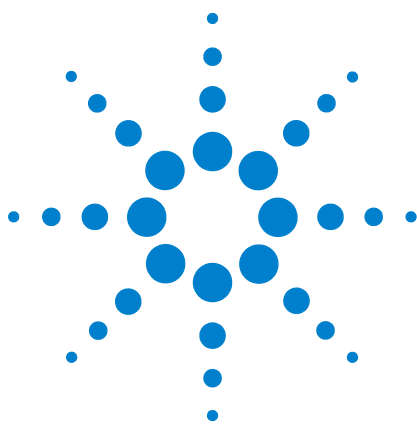
Two single-ended signals are probed independently, acquired simultaneously and compared.

PASS Condition

AC Common Mode Noise $\leq$ 20 mVrms.

Test References

See Test 3.10: AC Common Mode Noise, in the *DisplayPort-Compliance Test Specification Version 1.1*.



17 Link Layer Protocol Tests

Probing for Link Layer Protocol Tests 146

Link Layer Protocol Tests 147

This section provides the guidelines for link layer protocol tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application. Link layer protocol tests are not compliance tests. The purpose of these tests is to verify if the link layer protocol is operating properly prior to any tests. These tests verify if the DUT is able to respond well when the configuration of the link layer is changed.



Probing for Link Layer Protocol Tests

When performing the link layer protocol test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 46 below shows the single-ended connections for Link Layer Protocol Tests.

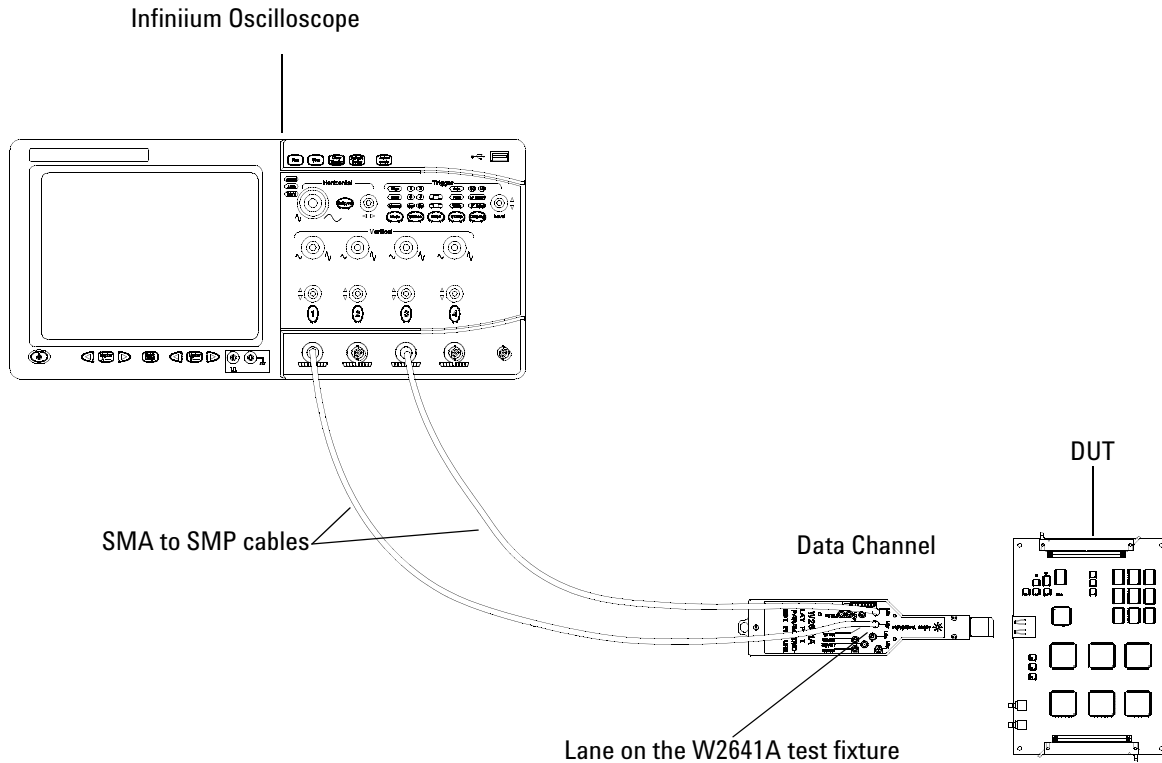


Figure 46 Differential Measurement Setup Using Two Single Ended Connections - Link Layer Protocol Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figure are just examples. You can choose any desired data lane and channel that you want.

Link Layer Protocol Tests

The link layer protocol tests consists of Pre-Emphasis, Level and Bit Rate tests.

Link Layer Protocol - Pre-Emphasis

The link layer - pre-Emphasis test verifies if the pre-Emphasis of the DUT can change accordingly from the lowest pre-Emphasis to the highest pre-Emphasis setting.

The test must be made on the highest bit rate supported by the differential voltage swings of 400 mV using a test pattern of PRBS 7. The following equation is used to calculate the pre-Emphasis result:

$$\text{Pre-Emphasis Result} = 20\log(\text{VSwingPE} / \text{VSwingNoPE})$$

$$\text{VSwingPE} = \text{VHpe} - \text{VLpe}$$

$$\text{VSwingNoPE} = \text{VHnope} - \text{VLnope}$$

where:

VHpe = the high voltage value is measured using the histogram modes at the top for transition eyes.

VLpe = the low voltage value is measured using the histogram modes at the top for transition eyes.

VHnope = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

VLnope = the high voltage value is measured using the histogram modes at the top for non-transition eyes.

Link Layer Protocol - Level

The link layer - level tests verifies if the amplitude level of the DUT can change accordingly from the lowest to the highest setting.

The amplitude measurement is performed using the following equation at all bit rates without pre-Emphasis and a PRBS 7 waveform:

$$\text{Peak-to-peak Voltage} = \text{VH} - \text{VL} \text{ where:}$$

VH is the high voltage level VL is the low voltage level

Link Layer Protocol - Bit Rate

The link layer - bit rate tests verifies if the bit rate of the DUT can change accordingly from the lowest to the highest setting.

The test must be made at all bit rates supported by the DUT without pre-Emphasis and a voltage swing of 400 mV. A test pattern of PRBS 7 should be used.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Fixture Type and Number of Channels according to the type of testing being done.

Navigate to the Link Layer (Protocol Test) group, and check the test and lane you want to test.

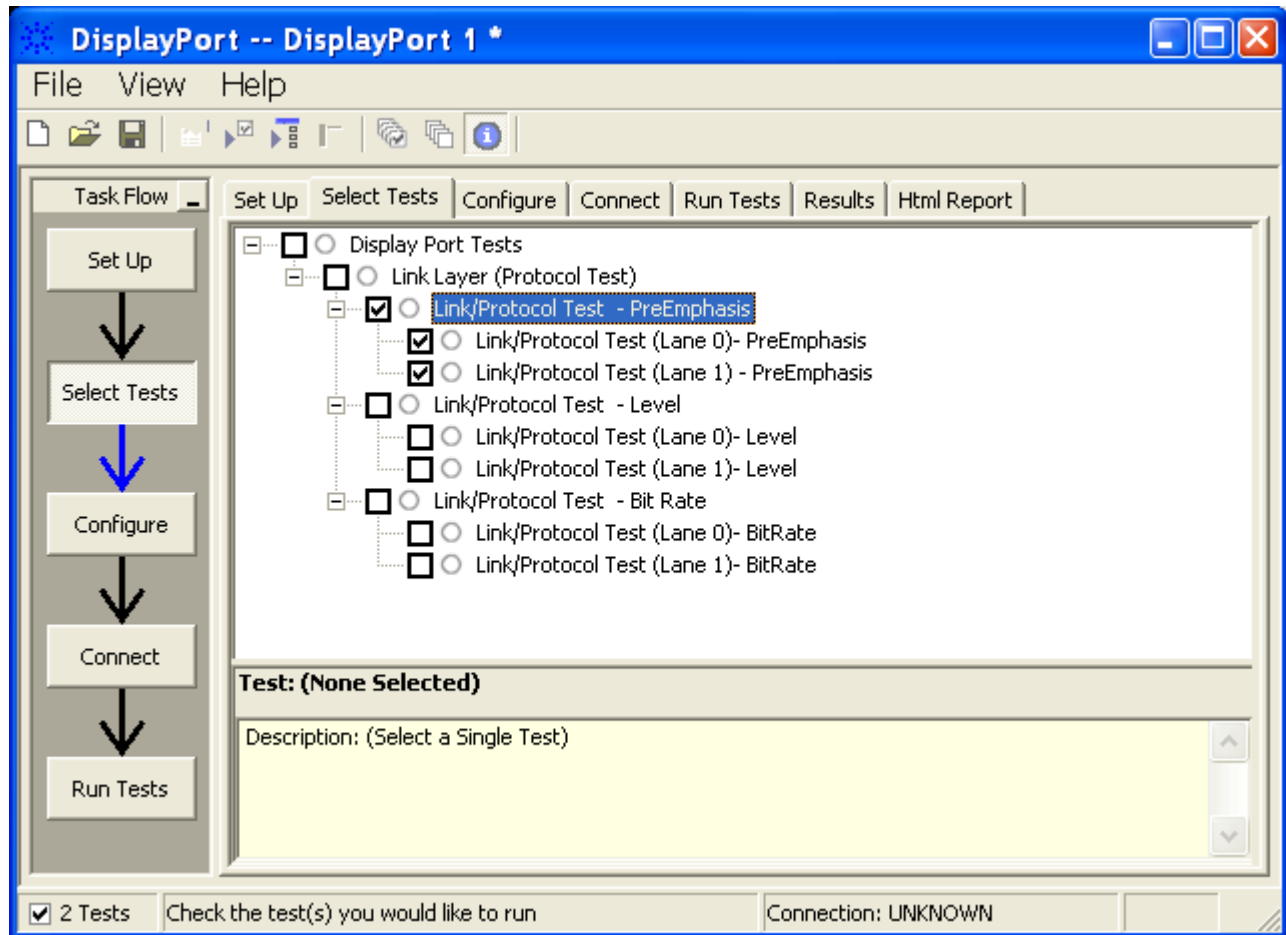


Figure 47 Selecting Link Layer Protocol Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 19](#)), make oscilloscope connections, run the tests, and view the tests results. Options may vary depending on the selected mode: Compliance Mode or Debug Mode.

Table 19 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 19 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
PRBS Validation Algorithm Settings	
PRBS pattern checker rule	Determine the rules applied to PRBS 7 Pattern detector. By selecting Strict, test can only proceed with the correct PRBS 7 pattern only.

Pre-Emphasis Test Condition

Bit Rate: highest bit rates are supported.

Output Level: 400 mVolts.

Pre-Emphasis: All.

Test Pattern: PRBS 7.

Level Test Condition

Bit Rate: highest bit rates are supported.

Output Level: All.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

Bit Rate Test Condition

Bit Rate: all bit rates are supported.

Output Level: 400 mVolts.

Pre-Emphasis: 0 dB.

Test Pattern: PRBS 7.

Pre-Emphasis PASS Condition

Link Layer Protocol - Pre-Emphasis Test

For 3.5 dB setting: $\text{Resultant}_{3.5\text{dB}} \geq 2.0 \text{ dB}$

For 6.0 dB setting: $\text{Resultant}_{6.0\text{dB}} \text{ results} \geq \text{Resultant}_{3.5\text{dB}} + 1.6$

For 9.5 dB setting: $\text{Resultant}_{9.5\text{dB}} \text{ results} \geq \text{Resultant}_{6.0\text{dB}} + 1.6$

Level PASS Condition

Link Layer Protocol - Level Test

Output Level 1: $340 \text{ mV} \leq \text{Voltage Peak-Peak} \leq 460 \text{ mV}$

Output Level 2: $510 \text{ mV} \leq \text{Voltage Peak-Peak} \leq 680 \text{ mV}$

Output Level 3: $690 \text{ mV} \leq \text{Voltage Peak-Peak} \leq 920 \text{ mV}$

Output Level 4: $1020 \text{ mV} \leq \text{Voltage Peak-Peak} \leq 1380 \text{ mV}$

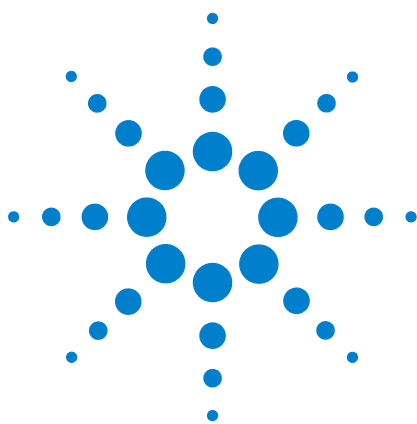
Bit Rate PASS Condition

Link Layer Protocol - Bit Rate Test

$0.9 * \text{Nominal Bit Rate} < \text{Measured Data Rate} < 1.1 * \text{Nominal Bit Rate}$

Test References

-



18 Sink Eye Diagram Tests

Probing for Sink Eye Diagram Tests [154](#)

Sink Eye Diagram Tests [156](#)

This section provides the guidelines for sink eye diagram tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Sink Eye Diagram Tests

When performing the sink eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 48 and Figure 49 show a physical connection for making differential and single-ended connections.

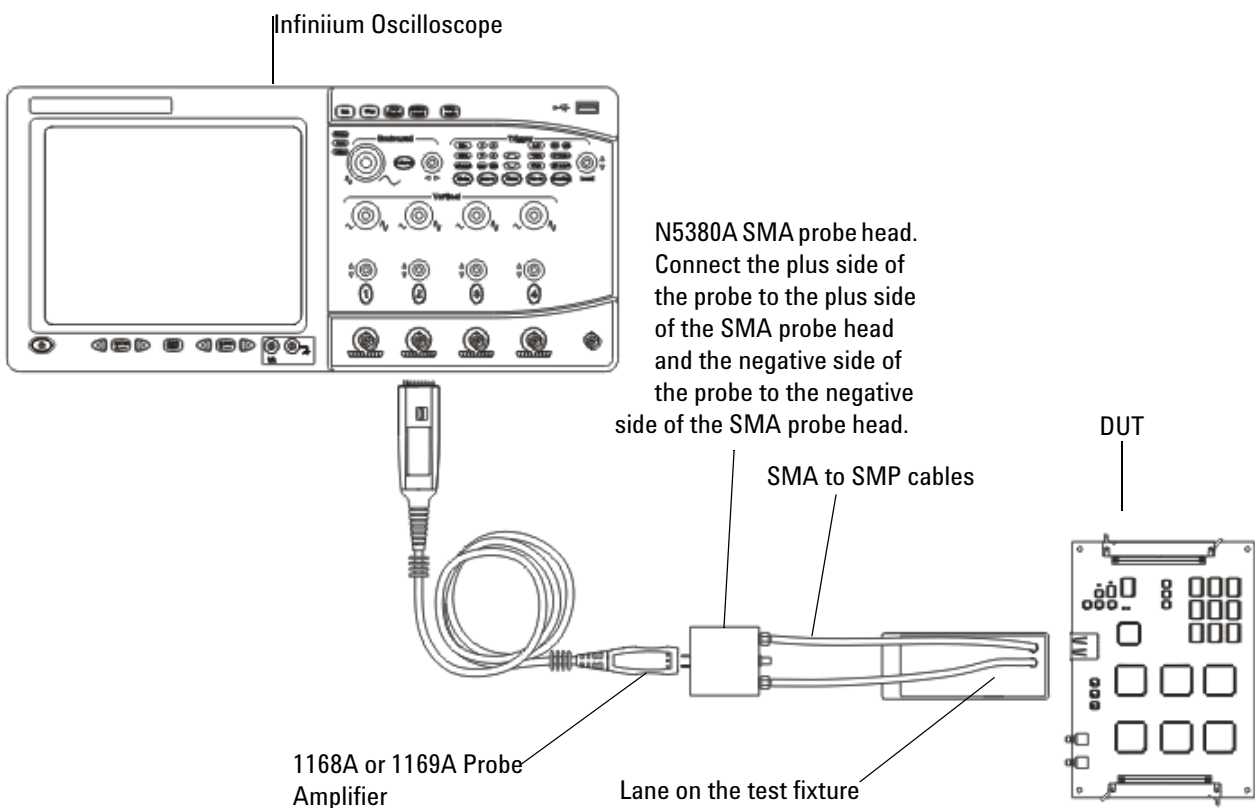


Figure 48 Probing for Differential Tests - Sink Eye Diagram Tests (Single Connection with DisplayPort Test Fixture)

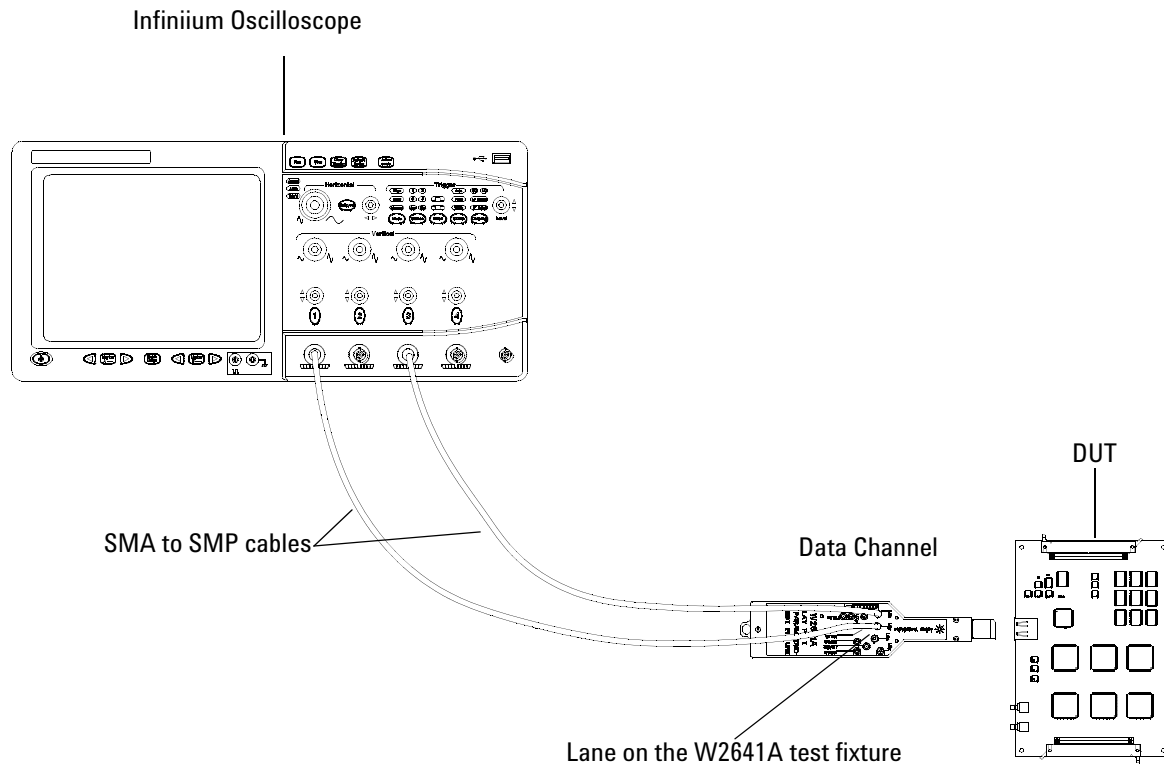


Figure 49 Differential Measurement Setup Using Two Single Ended Connections - Sink Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see [Chapter 25](#), “InfiniiMax Probing,” starting on page 231.

Sink Eye Diagram Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in the transmitted data. The test must use a PRBS 7 test pattern at all voltage levels. The test should be performed without pre-Emphasis.

The sink eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Eye Diagram Test - Lane # - Sink Eye Diagram Test where # is the lane number to be tested.

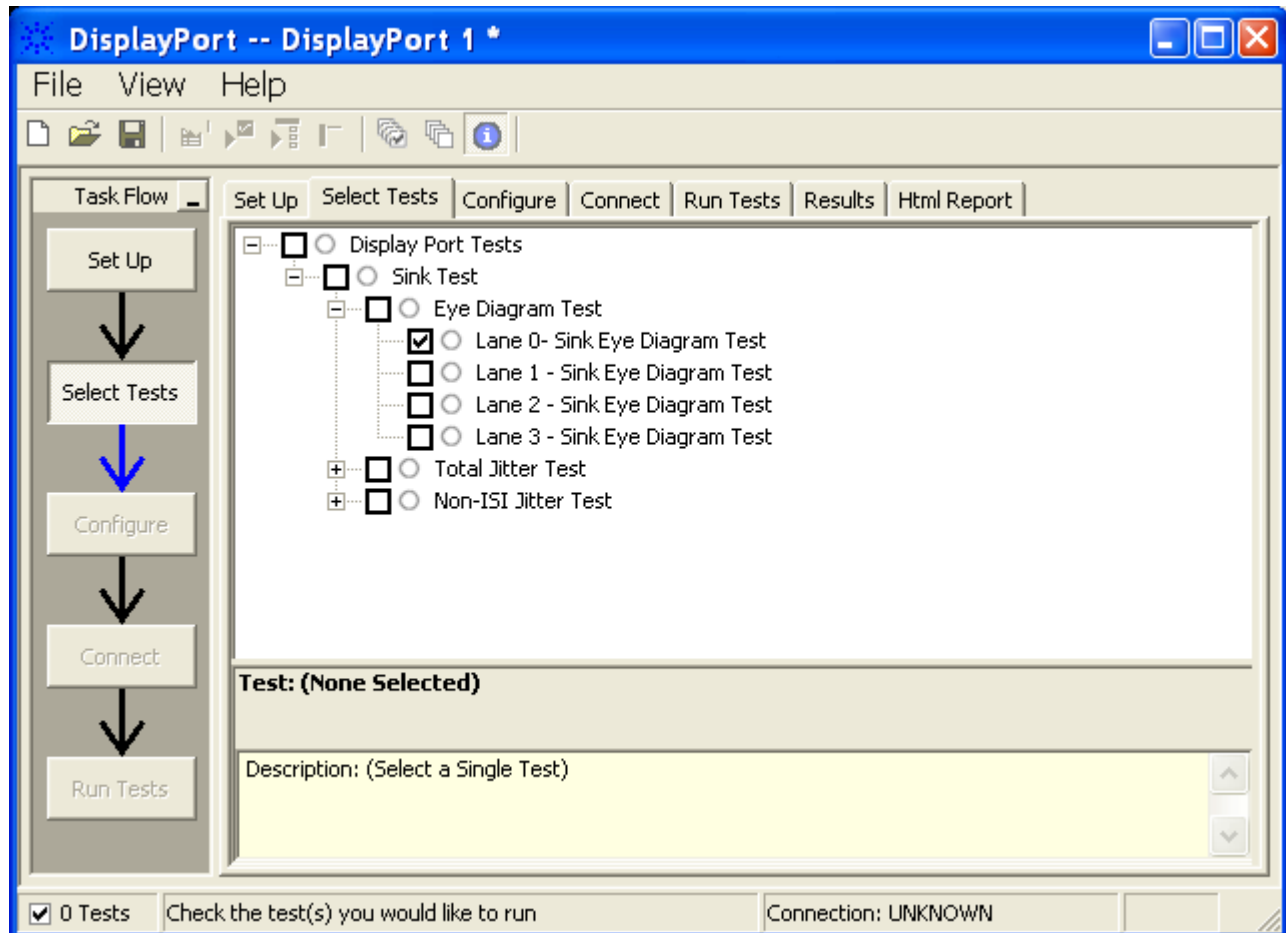


Figure 50 Selecting Sink Eye Diagram Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 20](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 20 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 20 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Sink Test	
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

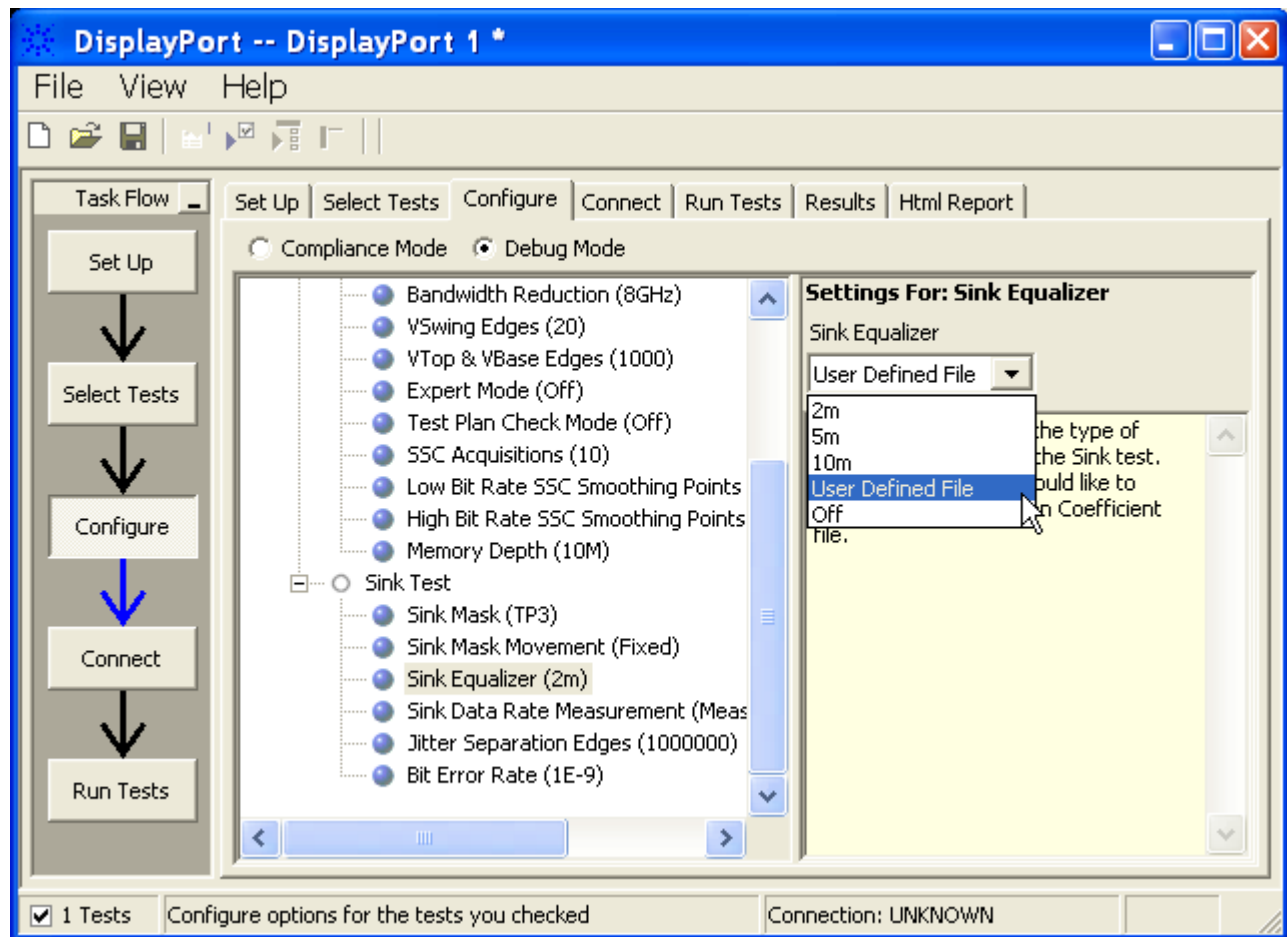


Figure 51 Selecting User Defined File for the Sink Equalizer

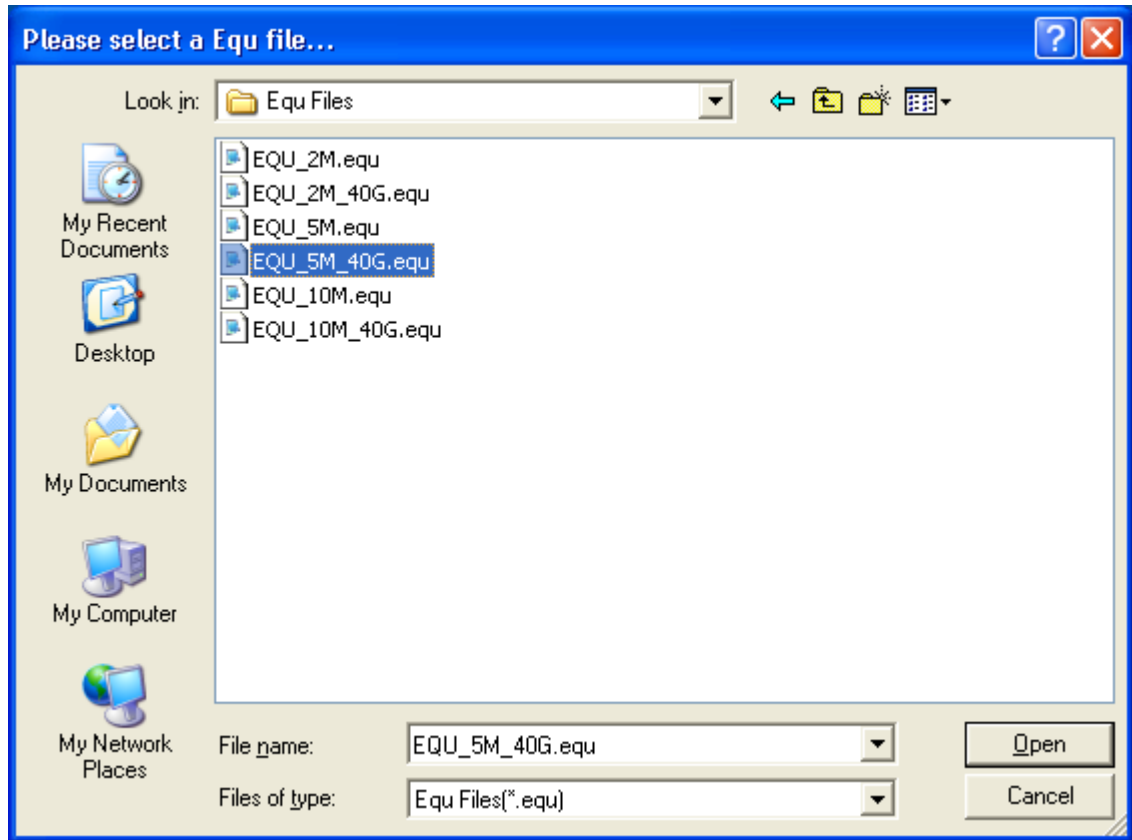


Figure 52 Selecting User Defined File

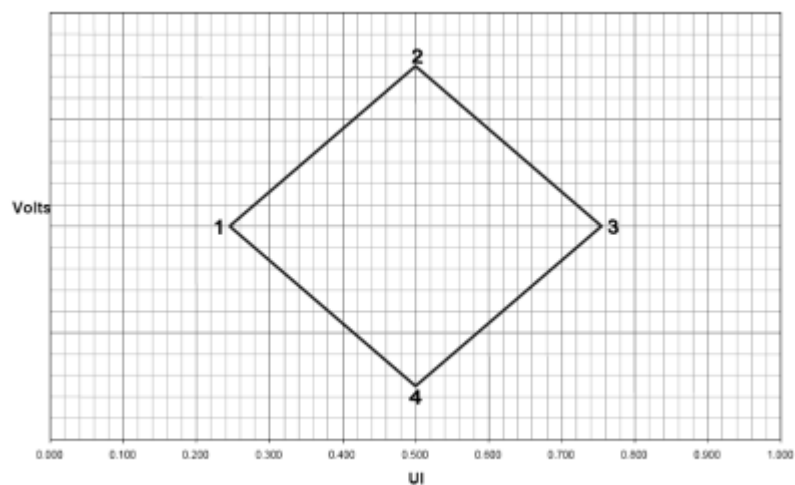
- 10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. [Table 21](#) shows the voltage and time coordinates for the mask used for the eye diagram.

Table 21 Sink Eye Vertices for TP3

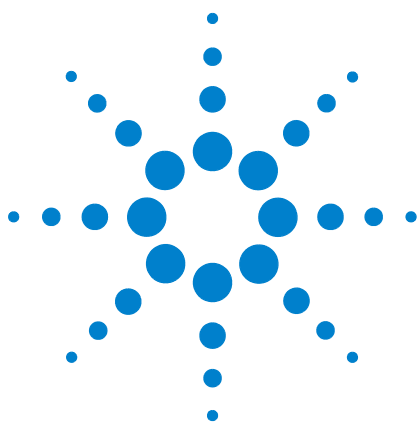
Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

**Figure 53** The Sink Eye Mask at TP3

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort-Compliance Test Specification Version 1.1*.



19 Sink Total Jitter Tests

Probing for Sink Total Jitter Tests [164](#)

Sink Total Jitter Tests [166](#)

This section provides the guidelines for sink total jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Sink Total Jitter Tests

When performing the sink total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 54 and Figure 55 show a physical connection for making differential and single-ended connections.

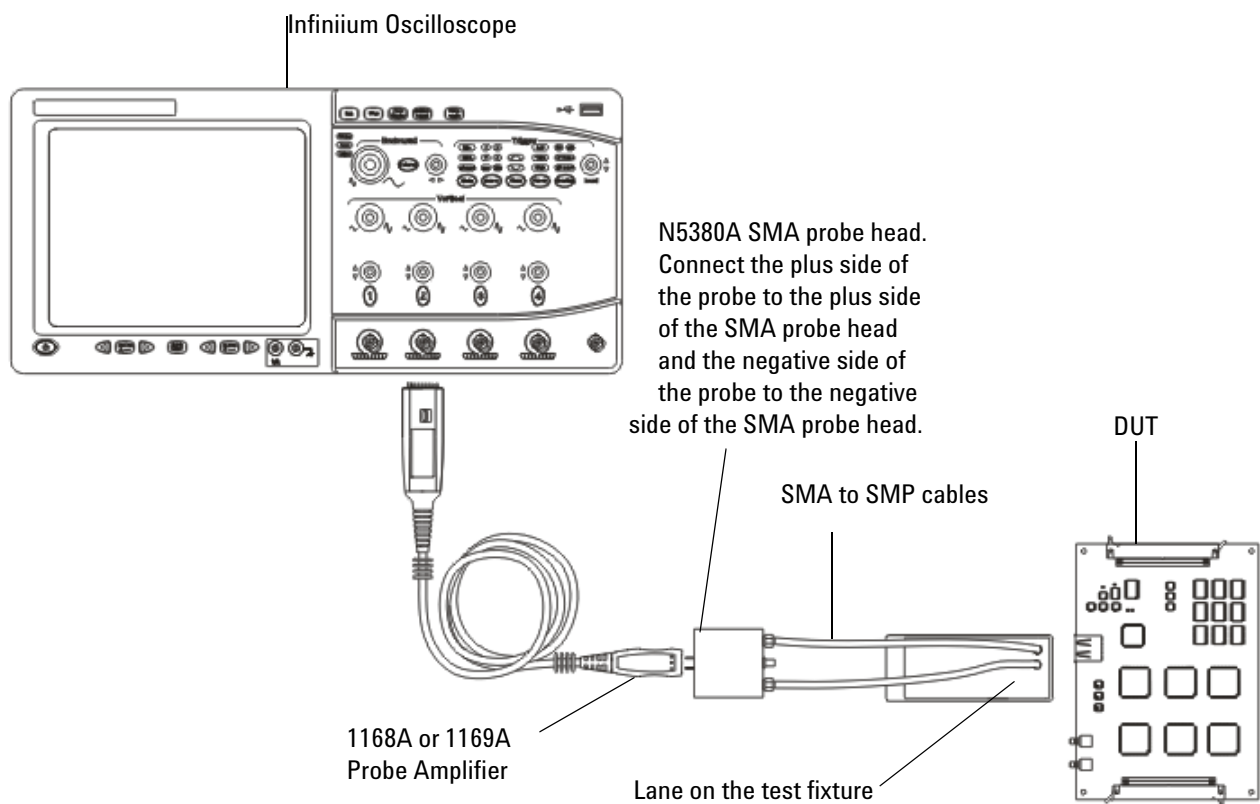


Figure 54 Probing for Differential Tests - Sink Total Jitter Tests (Single Connection with DisplayPort Test Fixture)

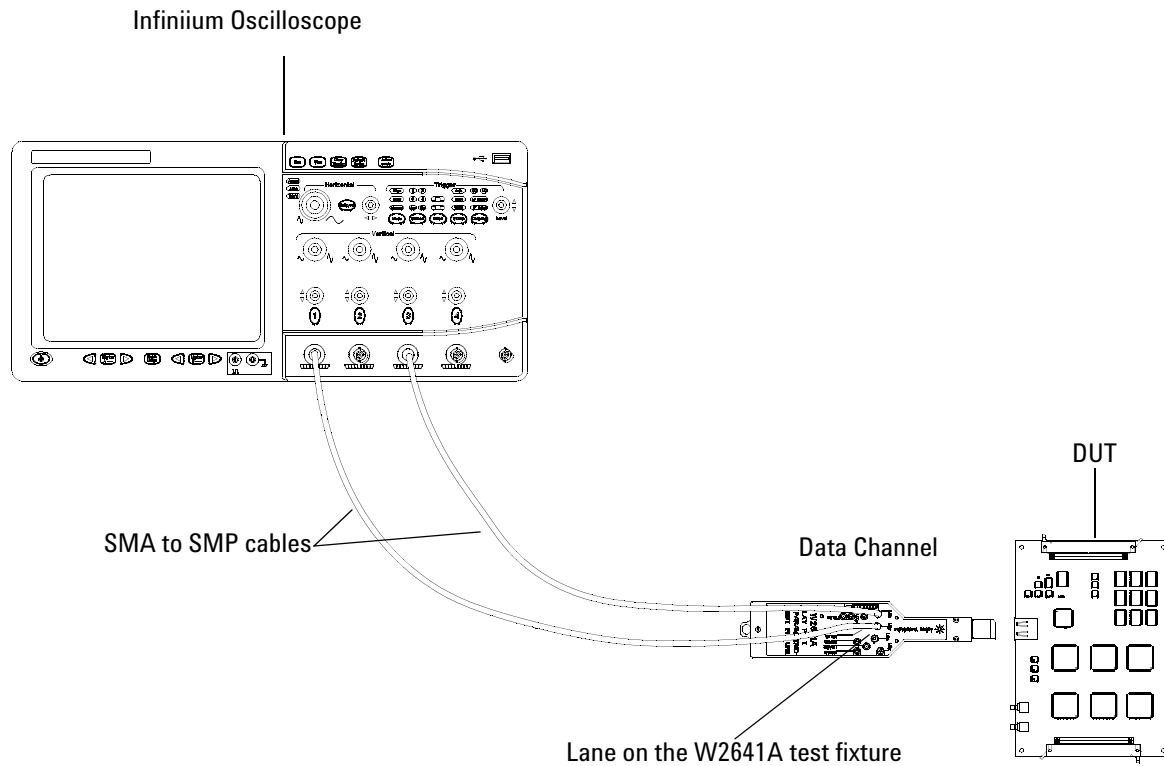


Figure 55 Differential Measurement Setup Using Two Single Ended Connections - Sink Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Sink Total Jitter Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Total Jitter Test - Lane # - Sink Total Jitter Test where # is the lane number to be tested.

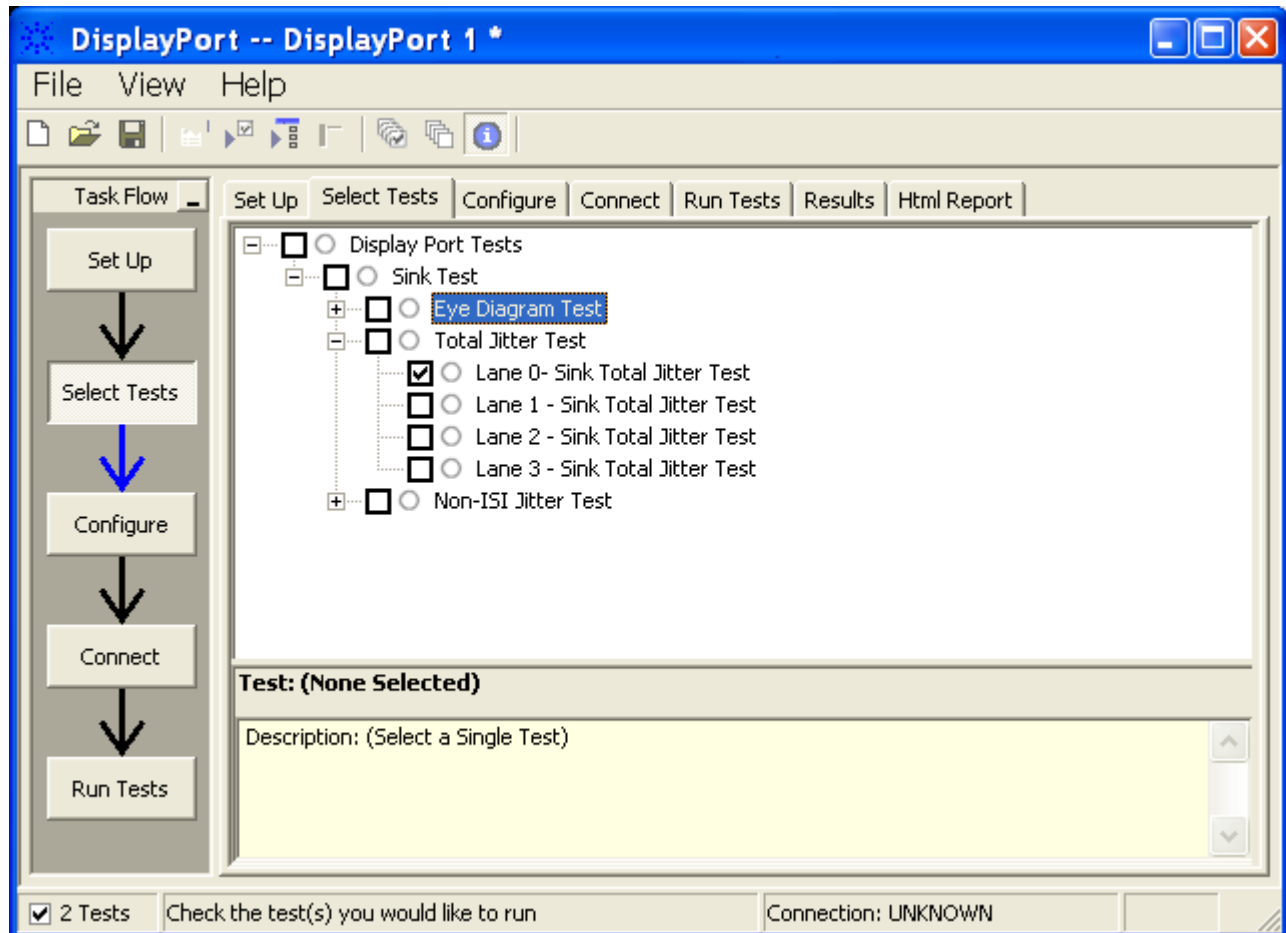


Figure 56 Selecting Sink Total Jitter Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 22](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 22 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 22 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Sink Test	
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

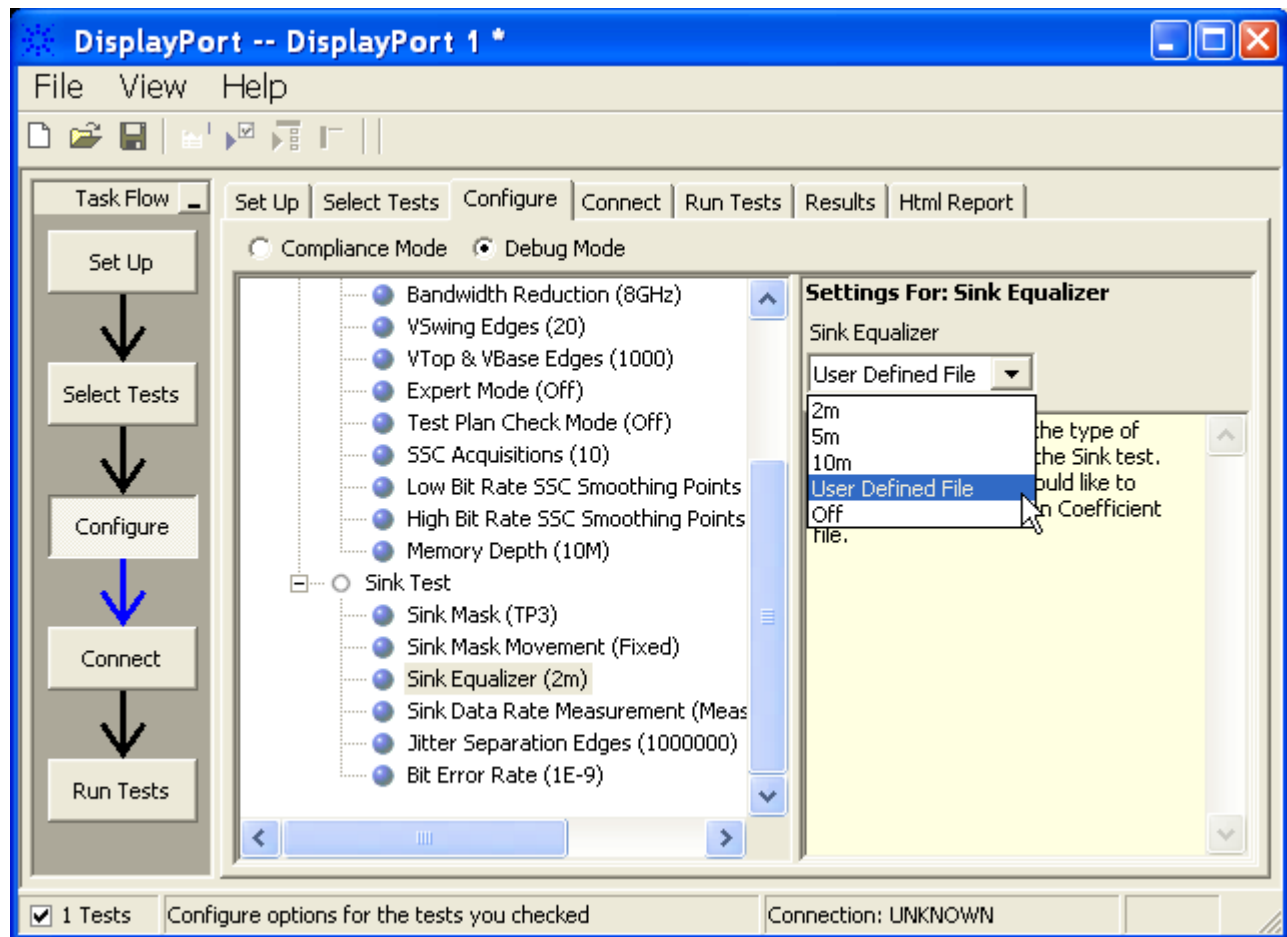


Figure 57 Selecting User Defined File for the Sink Equalizer

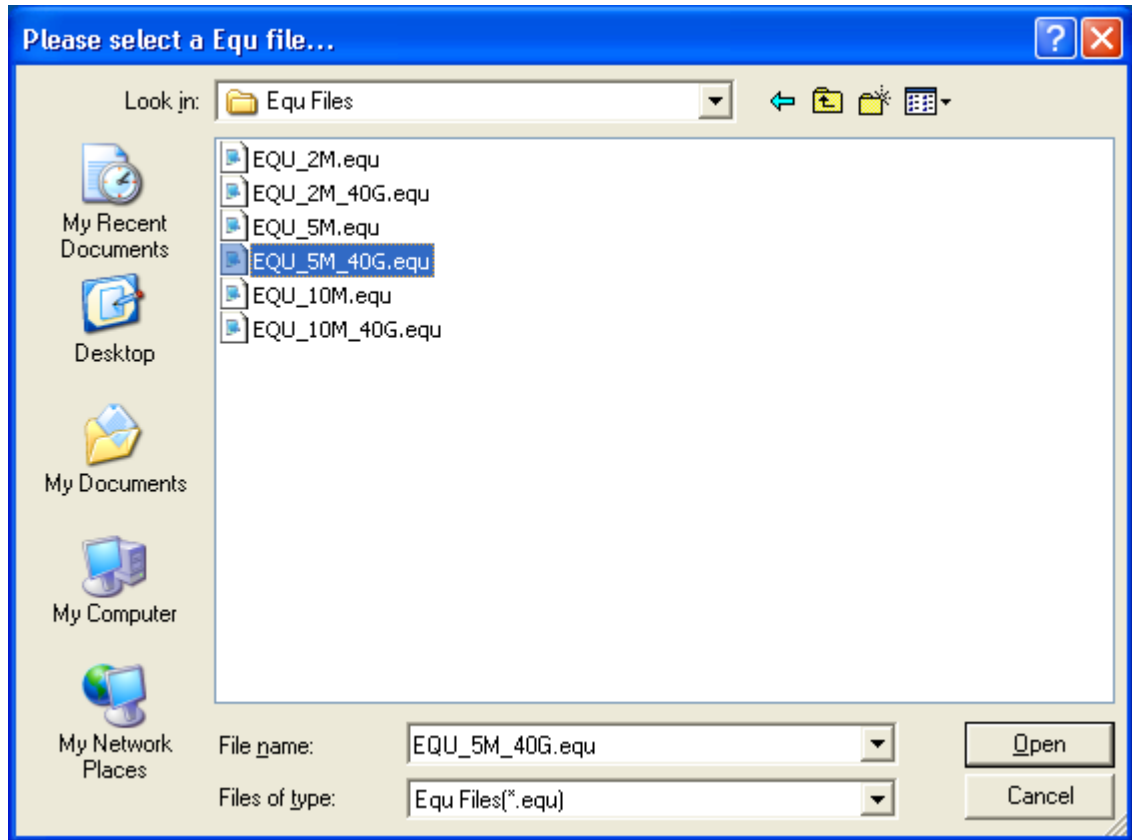


Figure 58 Selecting User Defined File

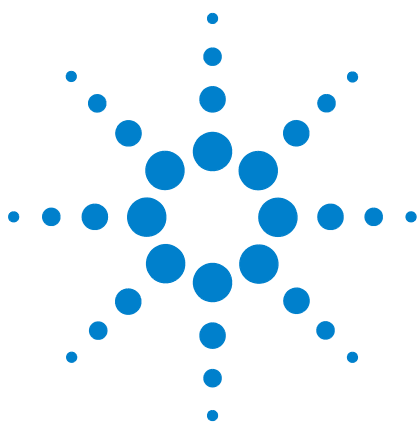
- 10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

-

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1.1*.



20

Sink Non-ISI Jitter Tests

Probing for Sink Non-ISI Jitter Tests [174](#)

Sink Non-ISI Jitter Tests [176](#)

This section provides the guidelines for sink non-ISI jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Sink Non-ISI Jitter Tests

When performing the sink non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 59 and Figure 60 show a physical connection for making differential and single-ended connections.

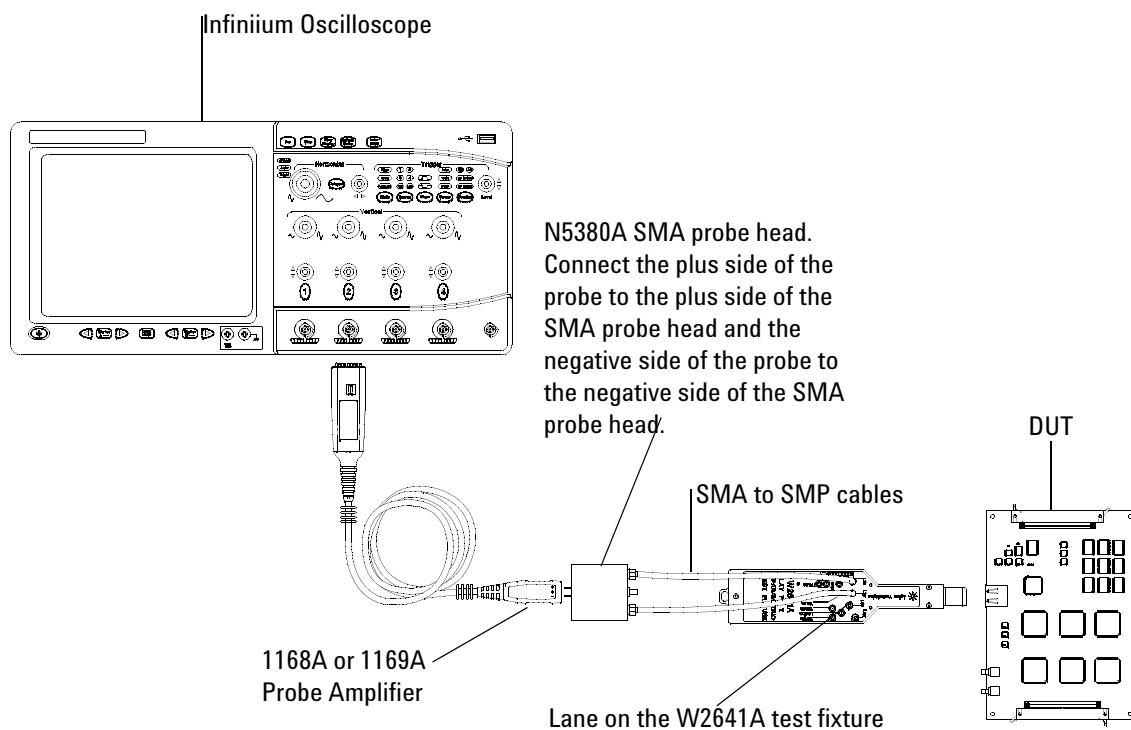


Figure 59 Probing for Differential Tests - Sink Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

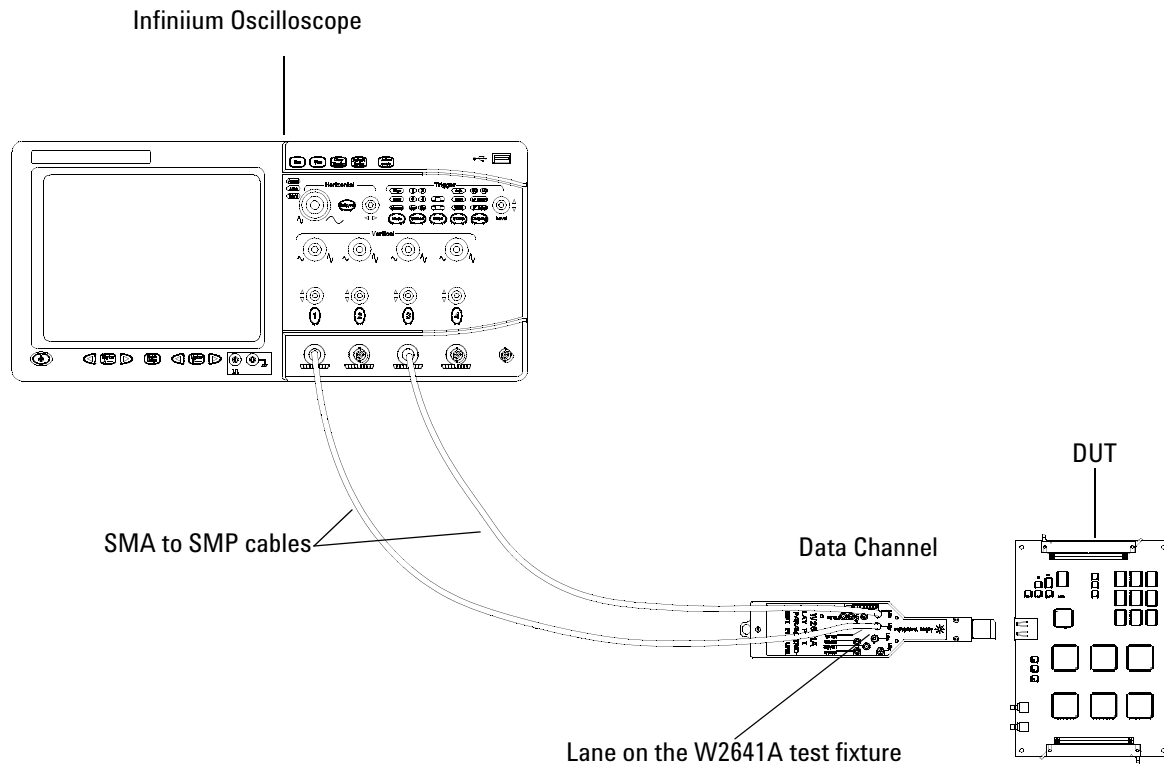


Figure 60 Differential Measurement Setup Using Two Single Ended Connections - Sink Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Sink Non-ISI Jitter Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Non-ISI Jitter Test - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

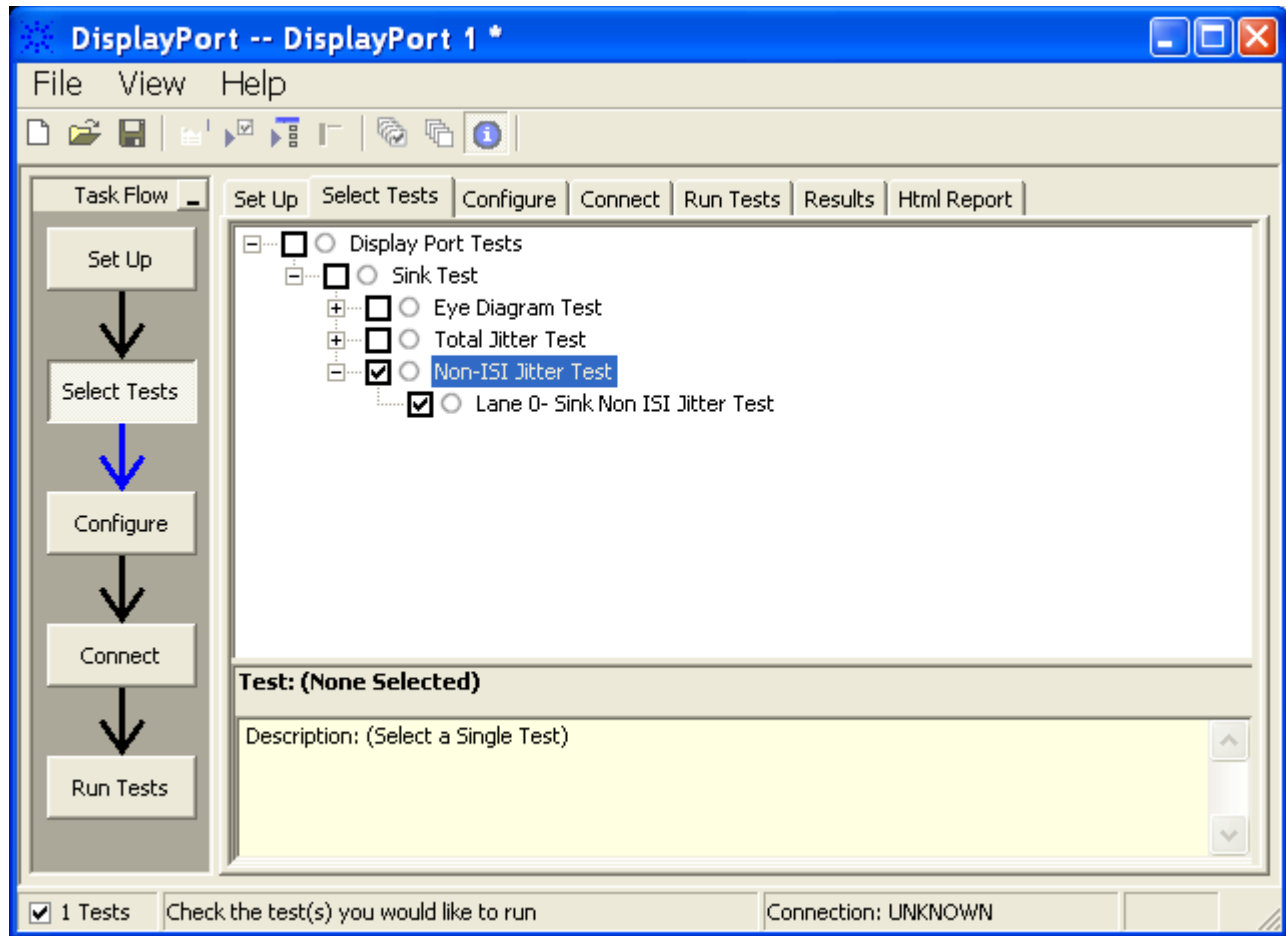


Figure 61 Selecting Sink Non-Jitter Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 23](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 23 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 23 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Sink Test	
Sink Mask	Selects the type of mask to use for the eye test.
Sink Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only reports Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Sink Equalizer	Selects the type of equalization to use for the Sink test. Select Manual if you would like to provide own Equalization Coefficient file.
Sink Data Rate Measurement	Specify the method to measure data rate on waveform. User can specifically enter the data rate by themselves.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Sink Equalizer option, Select “User Defined File” from the drop down menu.

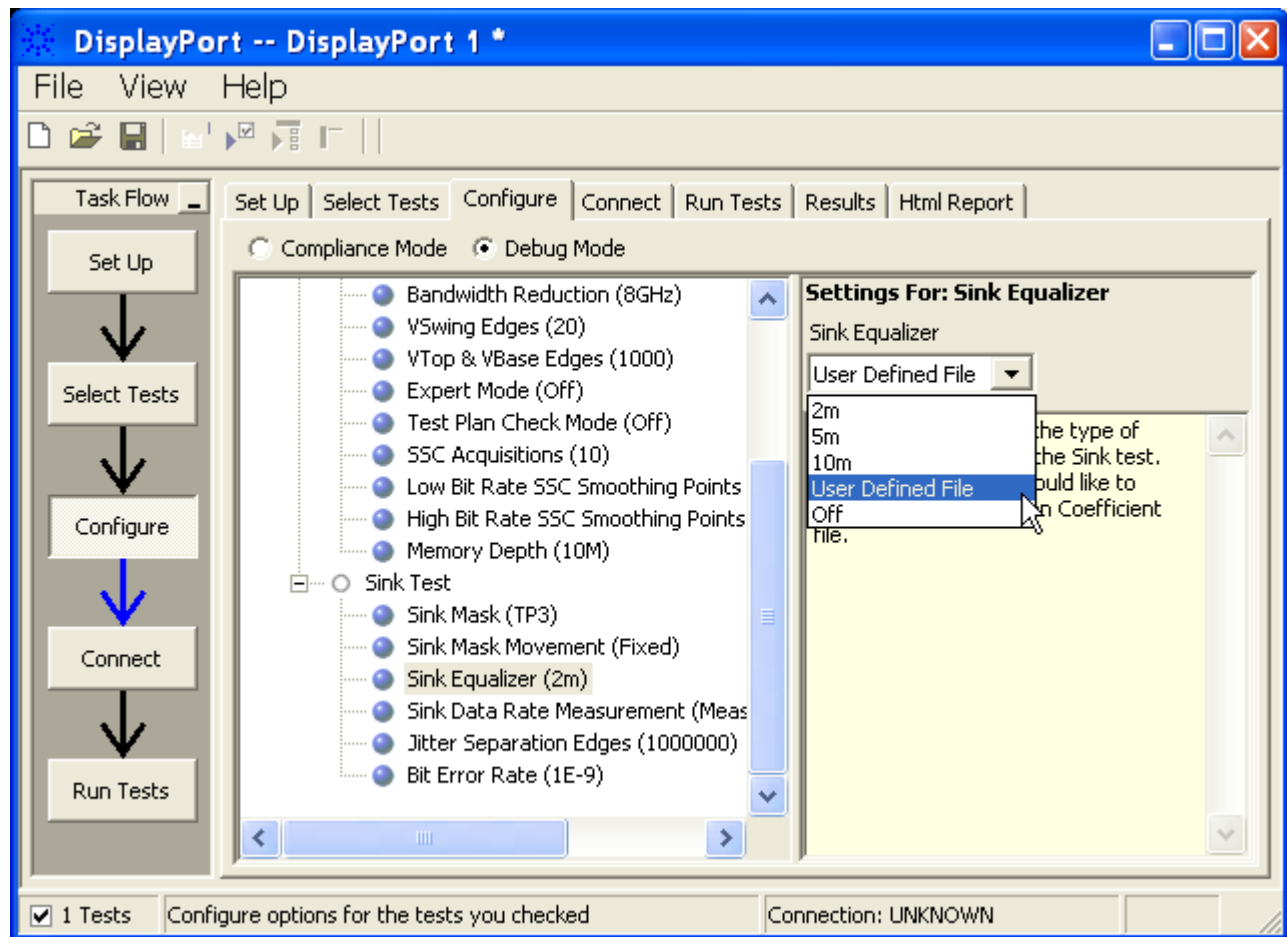


Figure 62 Selecting User Defined File for the Sink Equalizer

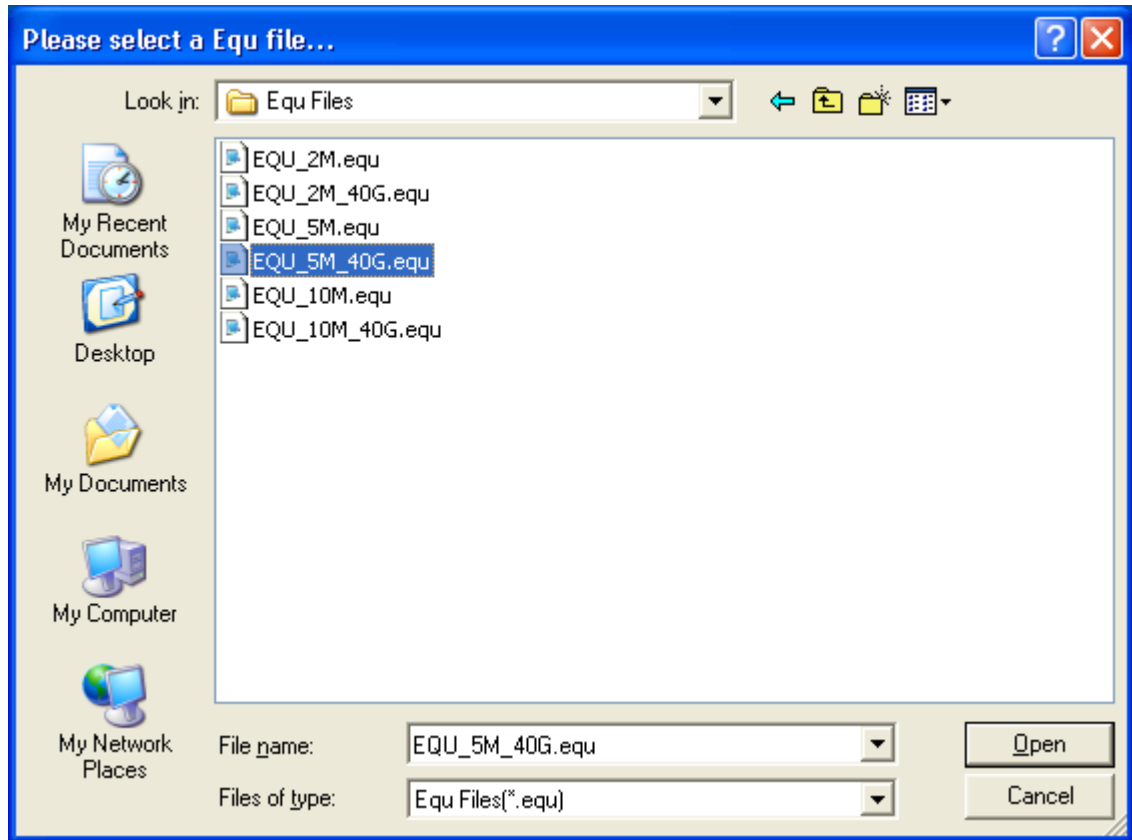


Figure 63 Selecting User Defined File

- 10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

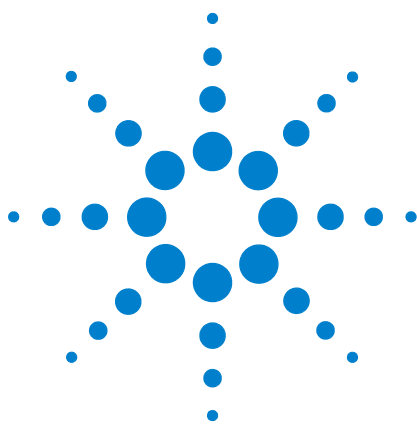
Table 24 Non-ISI Jitter at Internal and Compliance Points.

	Receiver package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.339 UI	0.330 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.465 UI	0.442 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the
DisplayPort-Compliance Test Specification Version 1.1.



21 Cable Eye Diagram Tests

Probing for Cable Eye Diagram Tests [184](#)

Cable Eye Diagram Tests [186](#)

This section provides the guidelines for cable eye diagram tests using an Agilent 8 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Cable Eye Diagram Tests

When performing the cable eye diagram test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 64 and Figure 65 show a physical connection for making differential and single-ended connections.

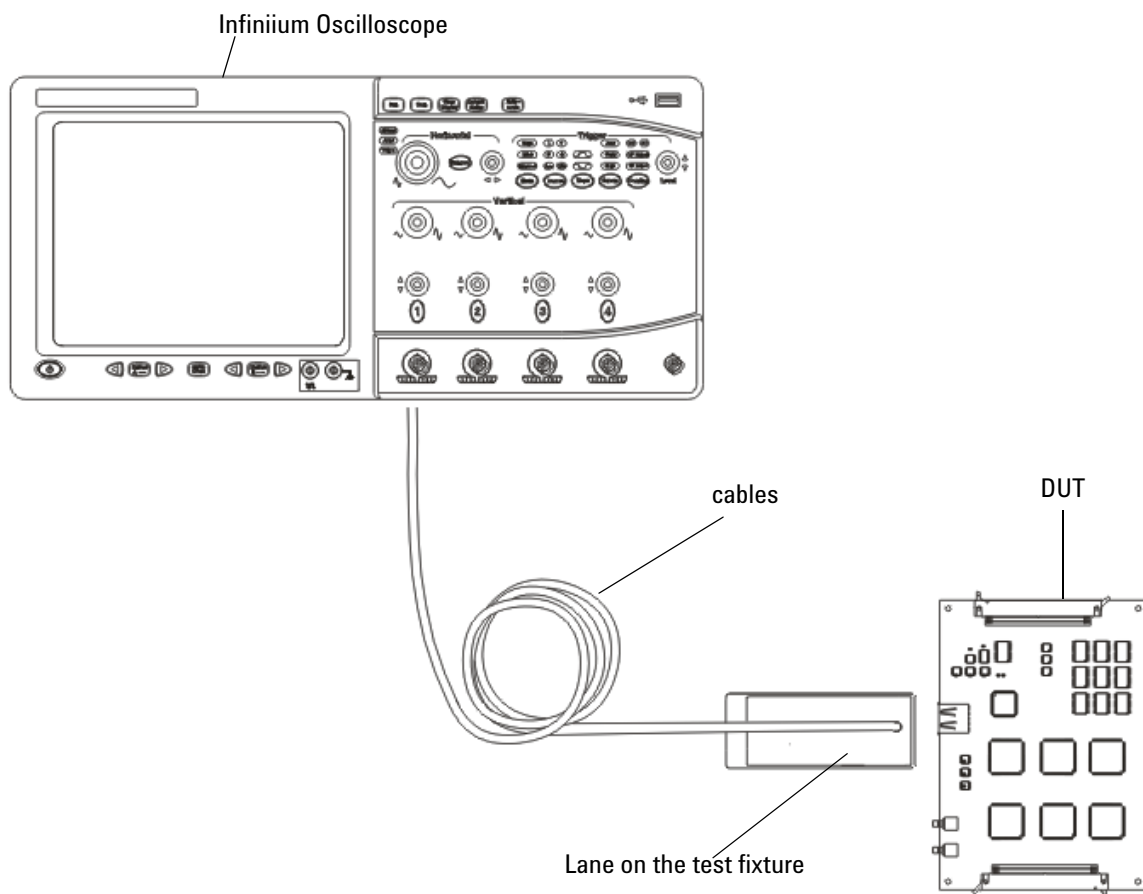


Figure 64 Probing for Differential Tests - Cable Eye Diagram Tests (Single Connection with DisplayPort Test Fixture)

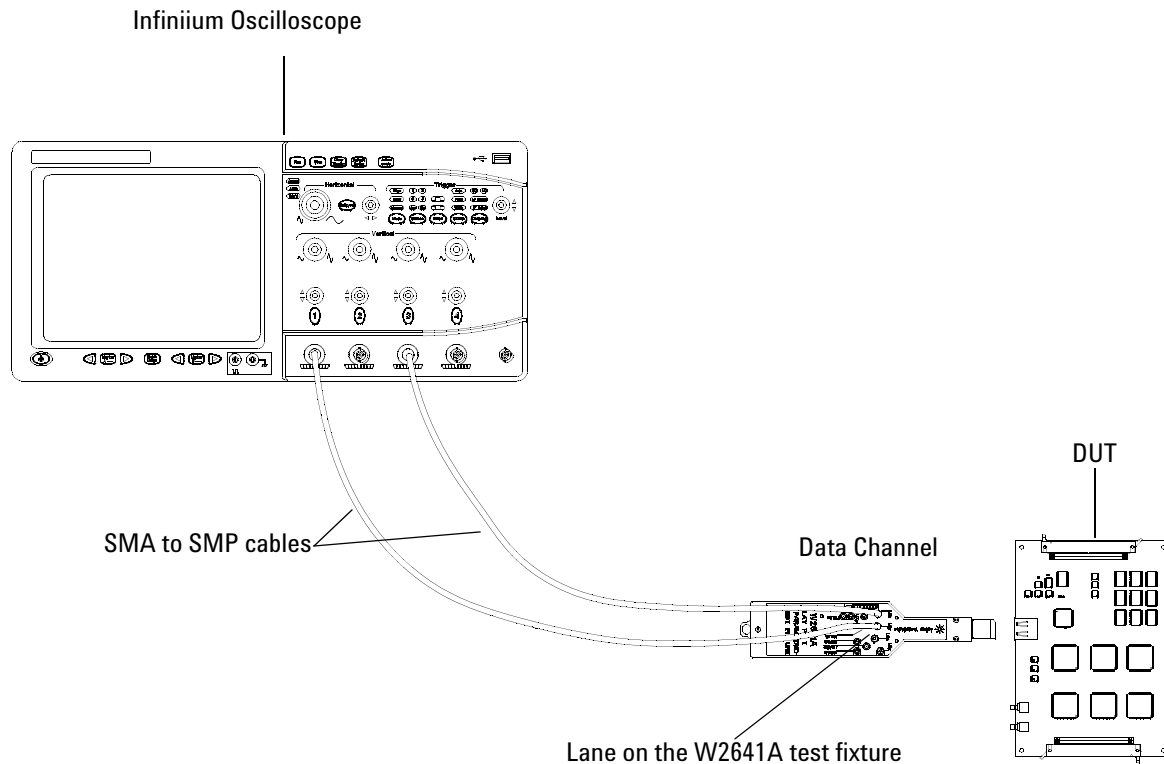


Figure 65 Differential Measurement Setup Using Two Single Ended Connections - Cable Eye Diagram Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

For more information on the 1168A or 1169A probe amplifiers and differential probe heads, see [Chapter 25](#), “InfiniMax Probing,” starting on page 231.

Cable Eye Diagram Tests

The eye diagram test provides a visual evaluation of the amplitude and timing variations of the waveform with the overall objective of obtaining a specified bit error rate in transmitted data. The test must use a PRBS 7 test pattern at all voltage levels. The test should be performed without pre-Emphasis.

The cable eye diagram performance provides the best visual assessment of interoperability potential by showing amplitude and timing minimum and maximum values.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Eye Diagram Test - Lane # - Cable Eye Diagram Test where # is the lane number to be tested.

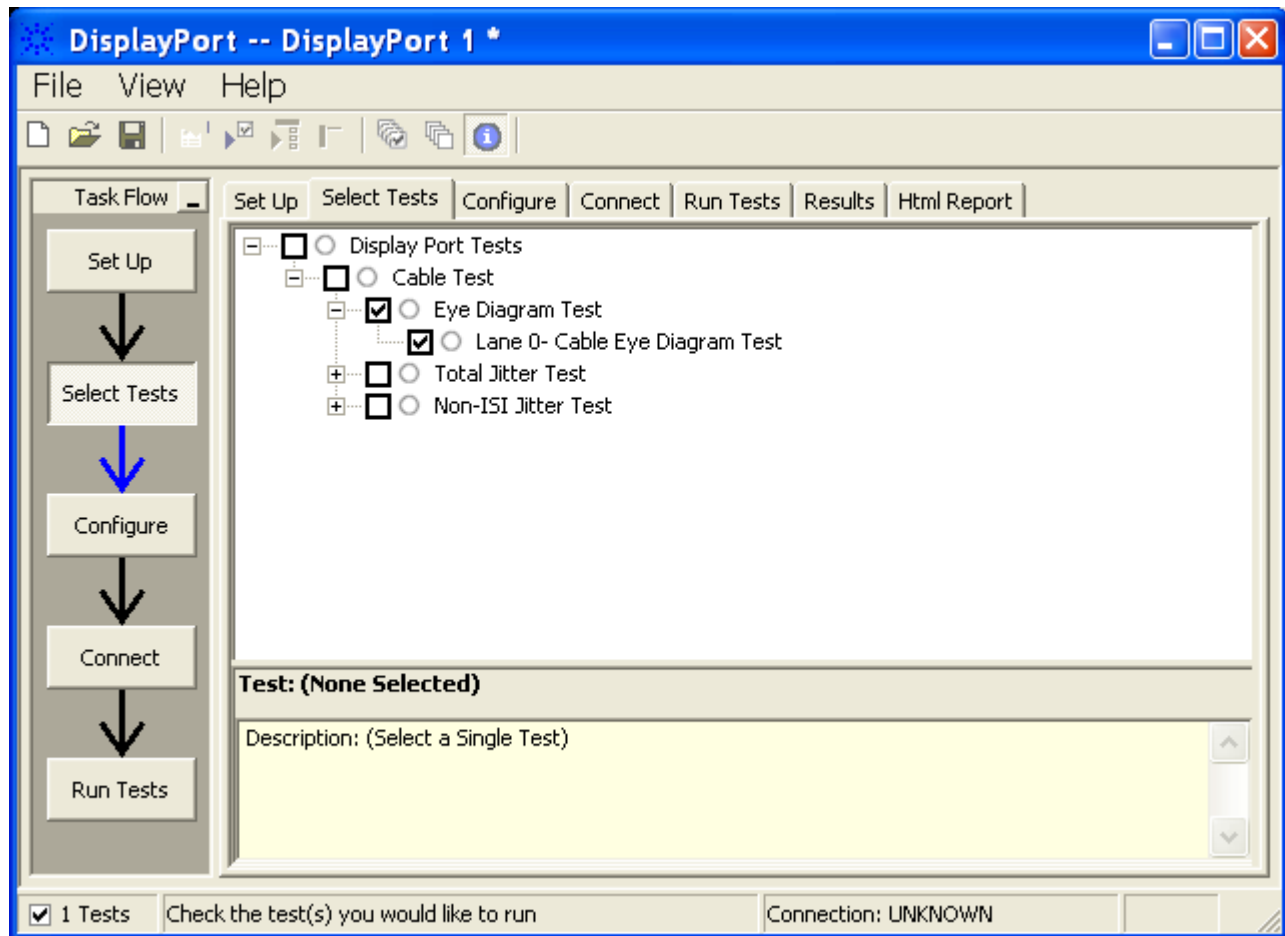


Figure 66 Selecting Cable Eye Diagram Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 25](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 25 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 25 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

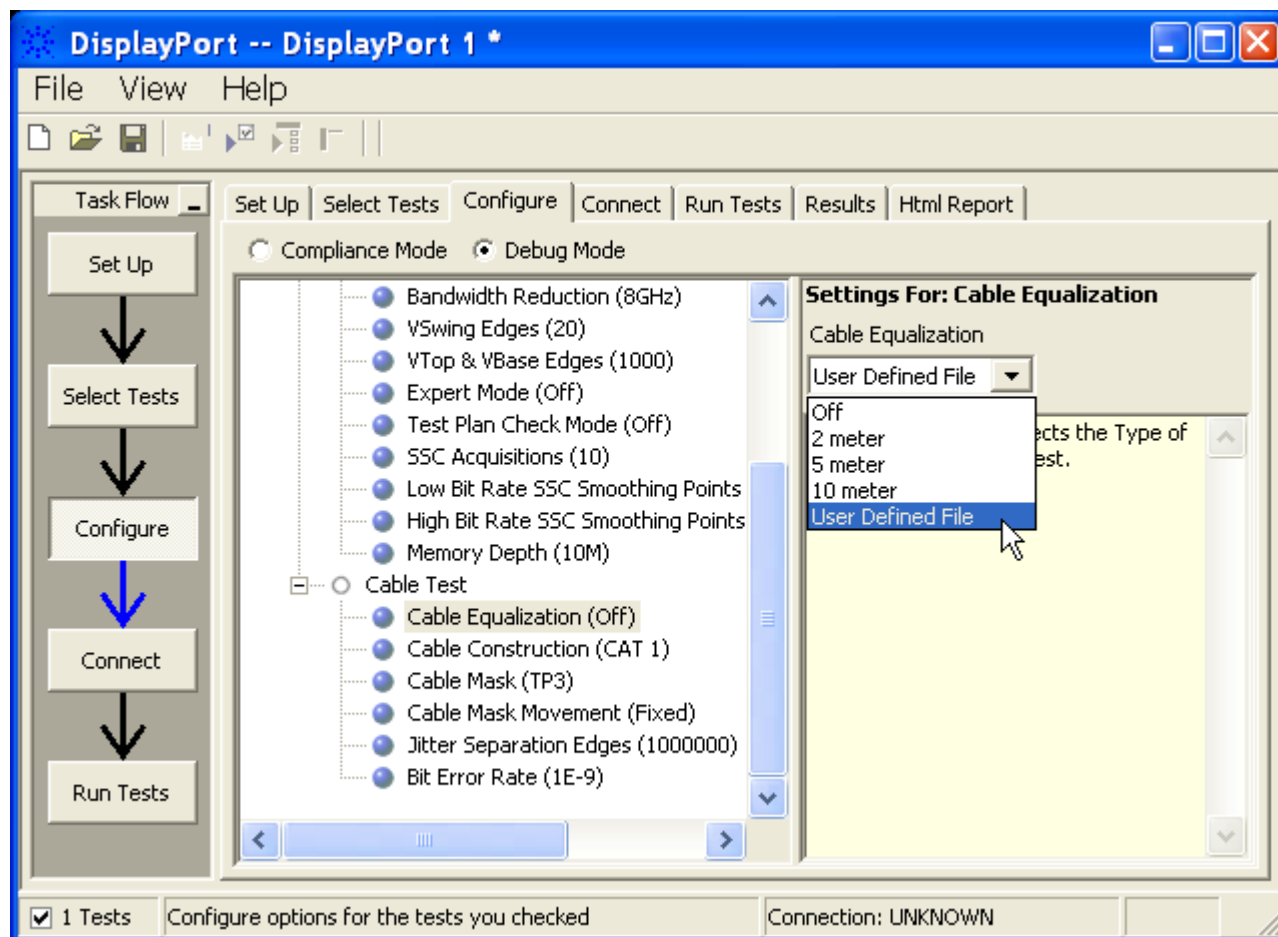


Figure 67 Selecting User Defined File for the Cable Equalizer

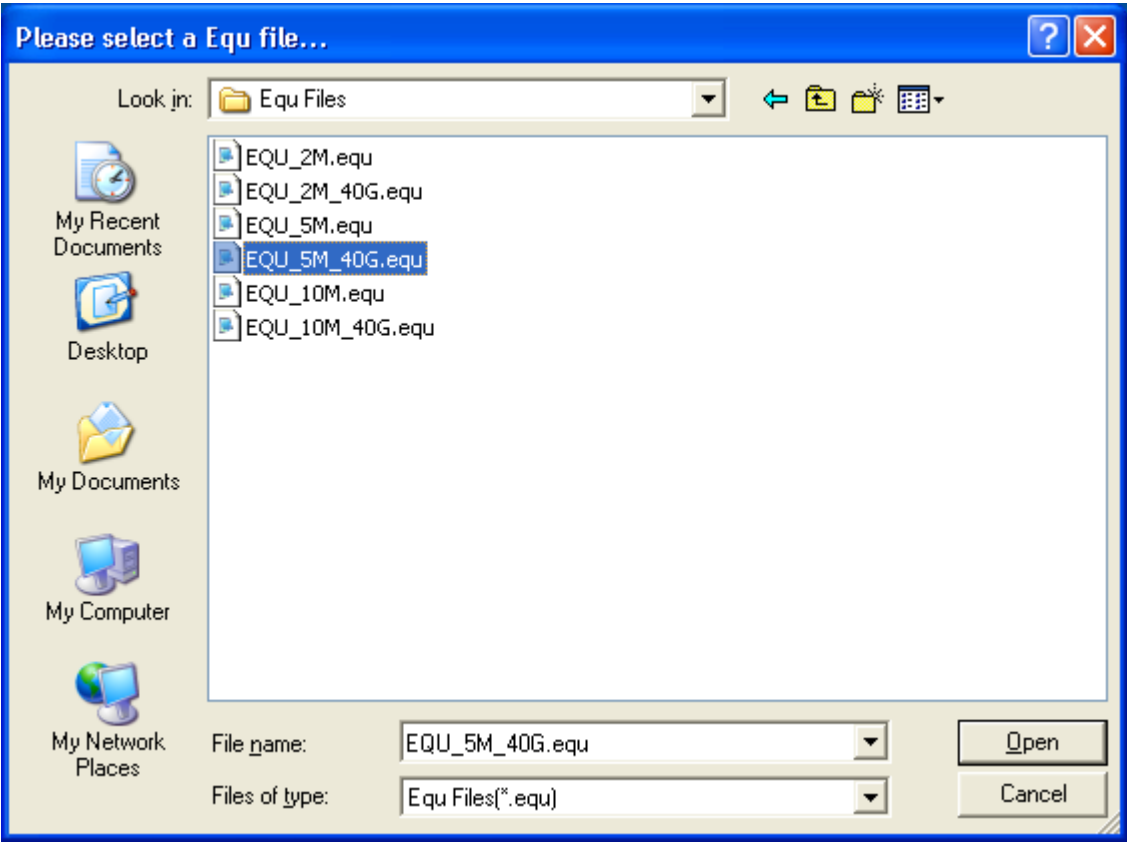


Figure 68 Selecting User Defined File

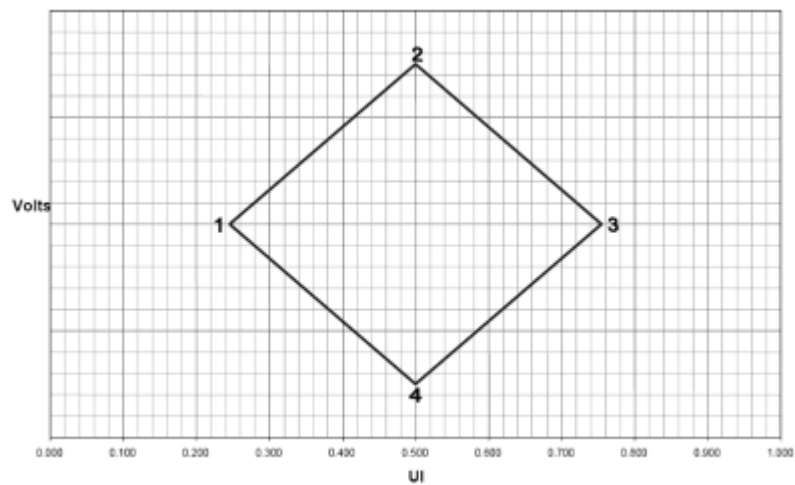
- 10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 26 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 26 Cable Eye Vertices for TP3

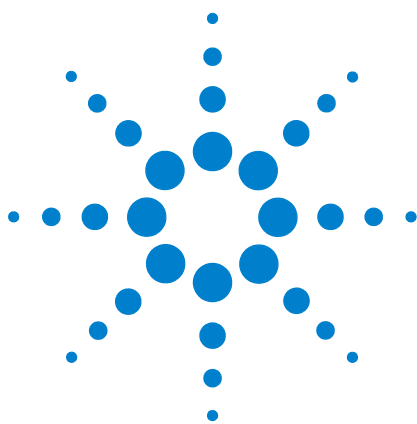
Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075


Figure 69 The Cable Eye Mask at TP3

Mask Test: Zero mask failures.

Test References

See Test 3.1: Eye Diagram Testing, in the *DisplayPort-Compliance Test Specification Version 1*.



22 Cable Total Jitter Tests

Probing for Cable Total Jitter Tests [194](#)

Cable Total Jitter Tests [196](#)

This section provides the guidelines for cable total jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Cable Total Jitter Tests

When performing the cable total jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 70 and Figure 71 show a physical connection for making differential and single-ended connections.

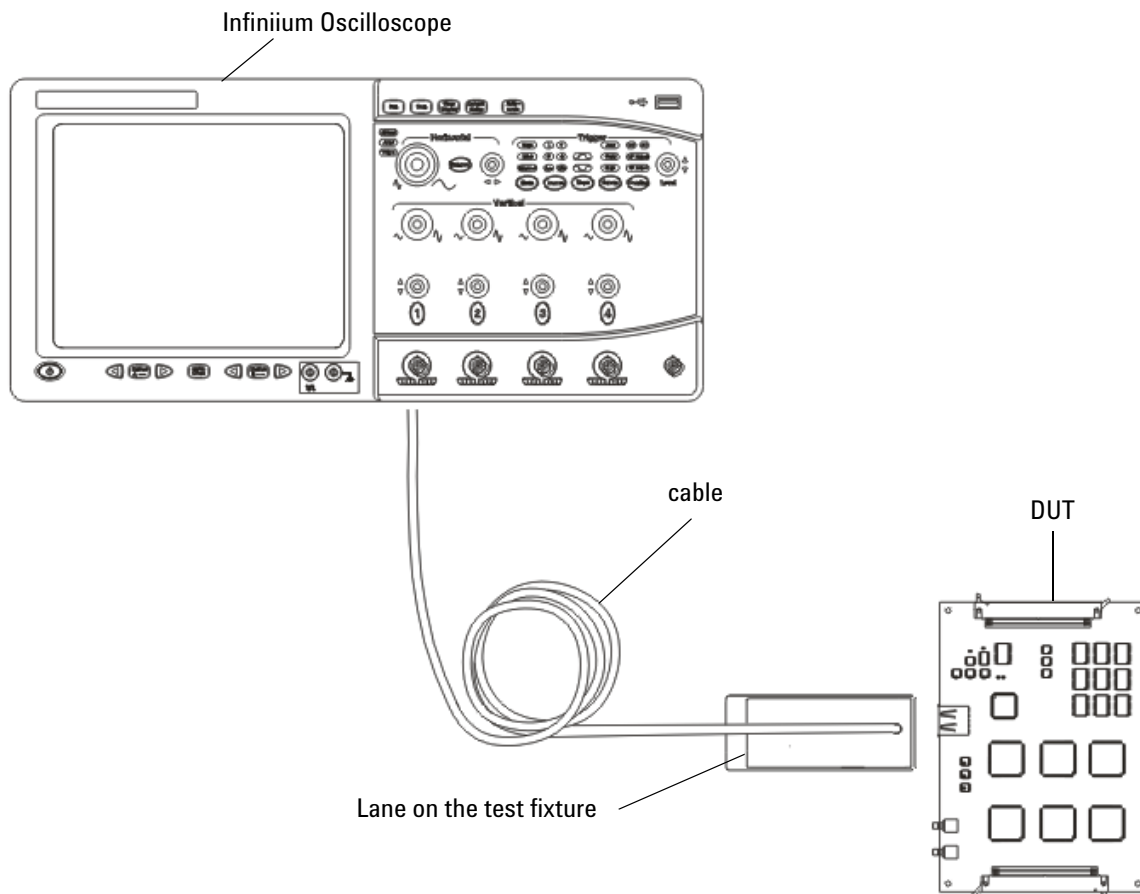


Figure 70 Probing for Differential Tests - Cable Total Jitter Tests (Single Connection with DisplayPort Test Fixture)

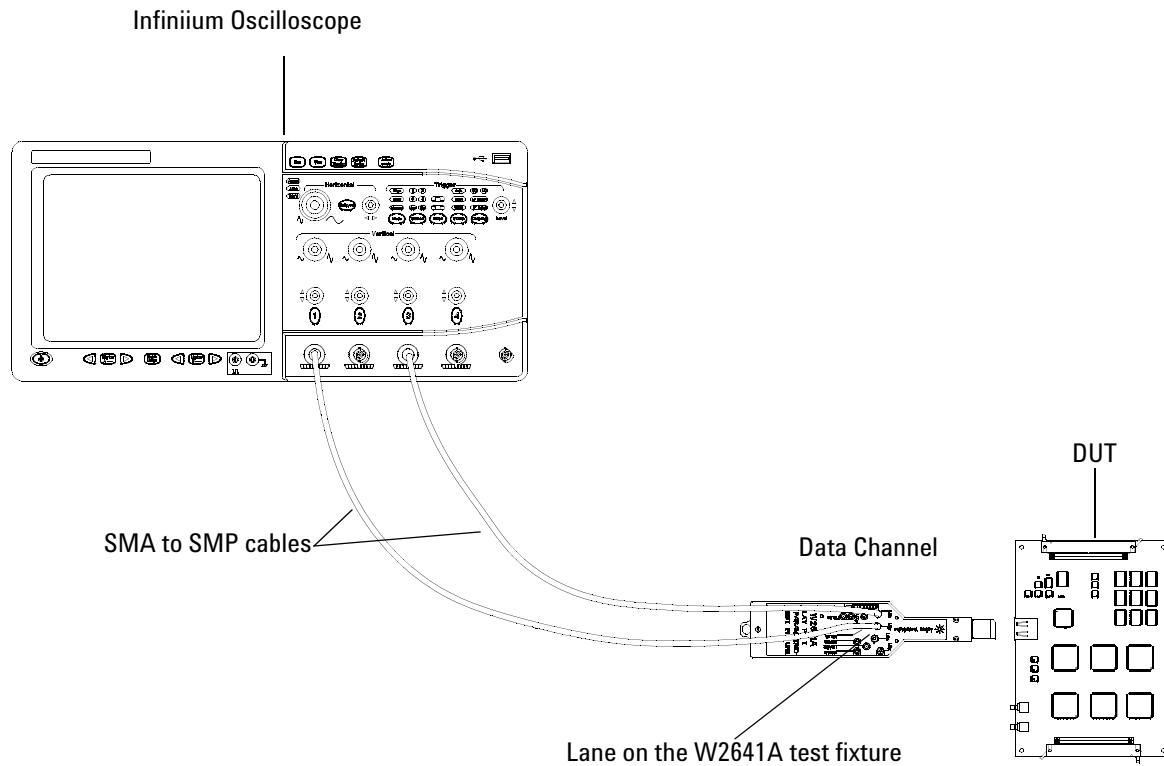


Figure 71 Differential Measurement Setup Using Two Single Ended Connections - Cable Total Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Cable Total Jitter Tests

To evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Total Jitter Test - Lane # - Cable Total Jitter Test where # is the lane number to be tested.

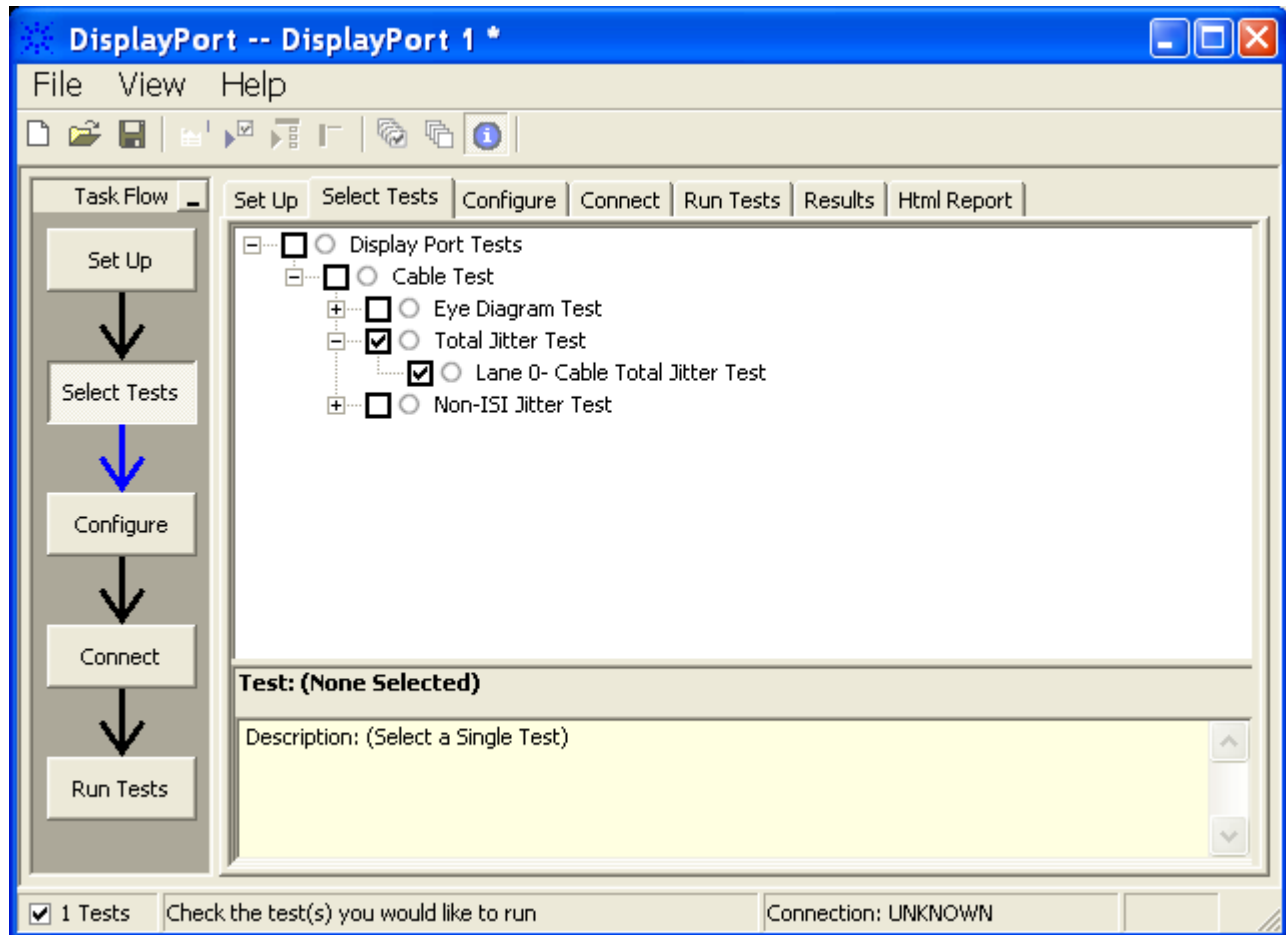


Figure 72 Selecting Cable Total Jitter Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 27](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 27 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 27 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

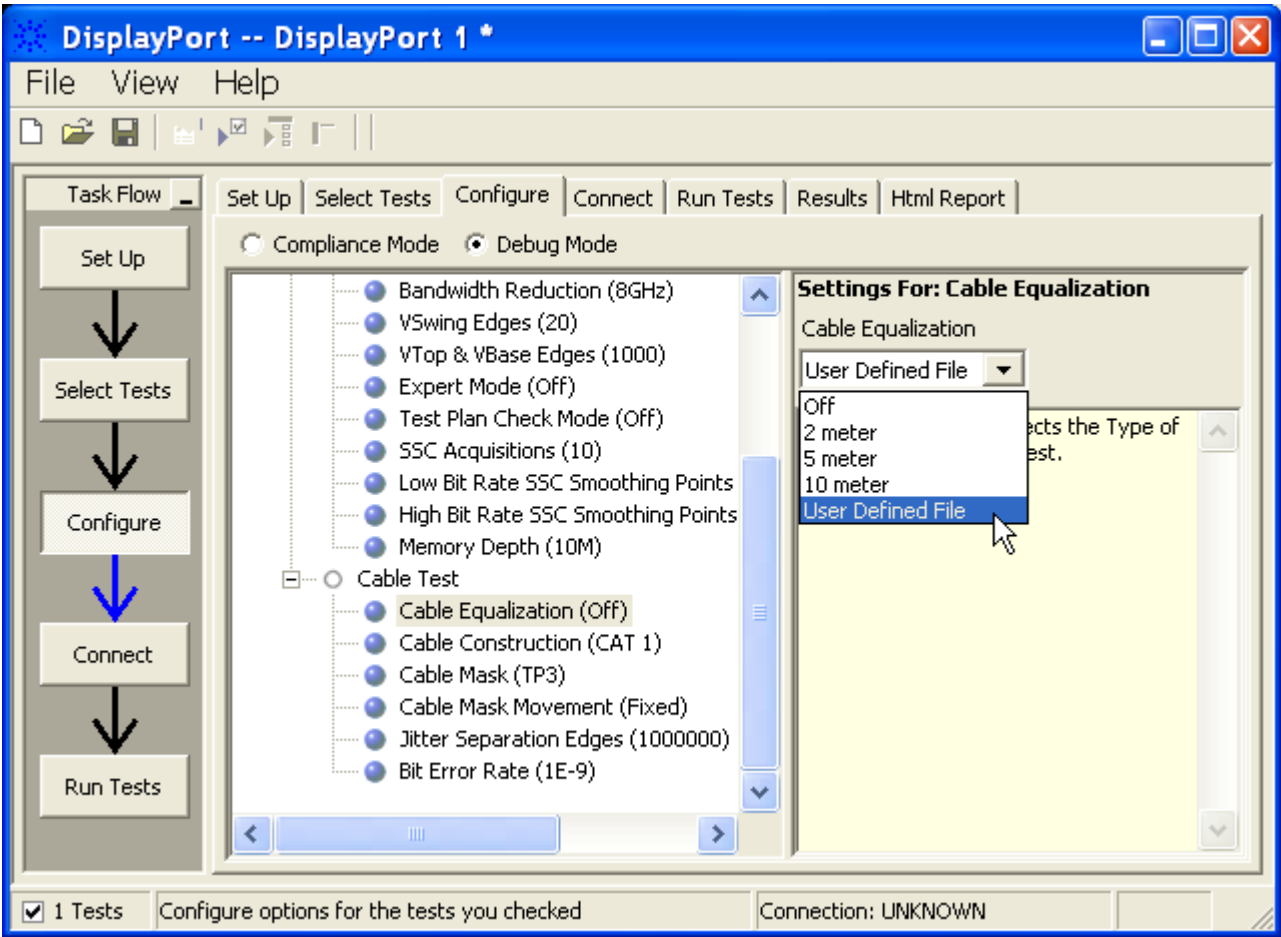


Figure 73 Selecting User Defined File for the Cable Equalizer

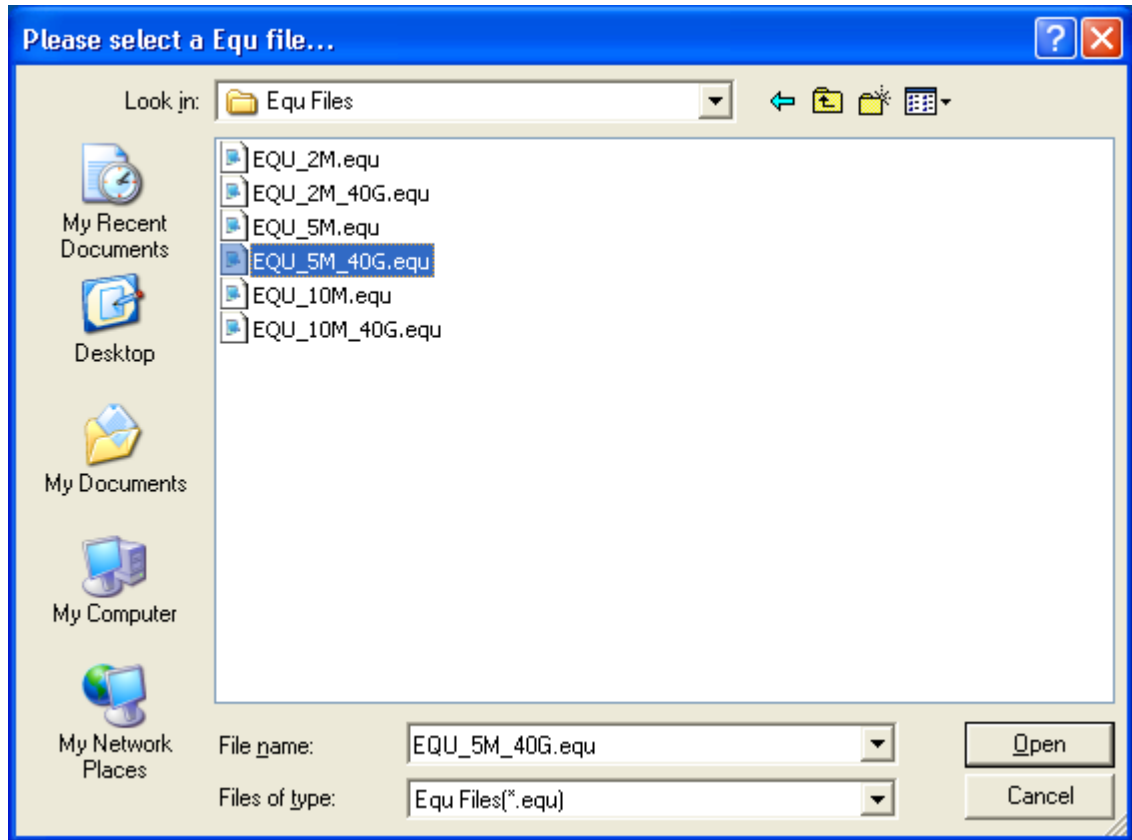


Figure 74 Selecting User Defined File

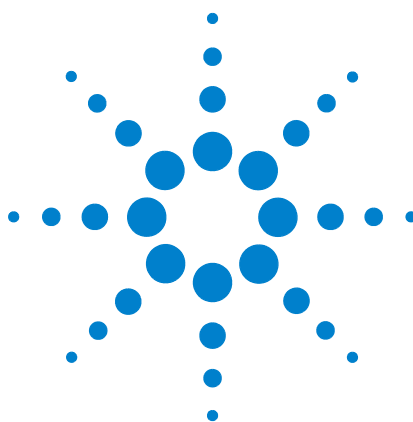
- 10 The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file.

PASS Condition

-

Test References

See Test 3.12: Total Jitter (TJ) Measurements in the *DisplayPort- Compliance Test Specification Version 1*.



23

Cable Non-ISI Jitter Tests

Probing for Cable Non-ISI Jitter Tests [204](#)

Cable Non-ISI Jitter Tests [206](#)

This section provides the guidelines for cable non-ISI jitter tests using an Agilent 8 GHz or greater Infiniium oscilloscope, InfiniiMax probes, and the DisplayPort Electrical Performance Compliance Test Application.



Probing for Cable Non-ISI Jitter Tests

When performing the cable non-ISI jitter test, the DisplayPort Electrical Performance Compliance Test Application will prompt you to make the proper connections. Your DisplayPort test environment setup on the Set Up tab must match the physical connection.

Figure 75 and Figure 76 show a physical connection for making differential and single-ended connections.

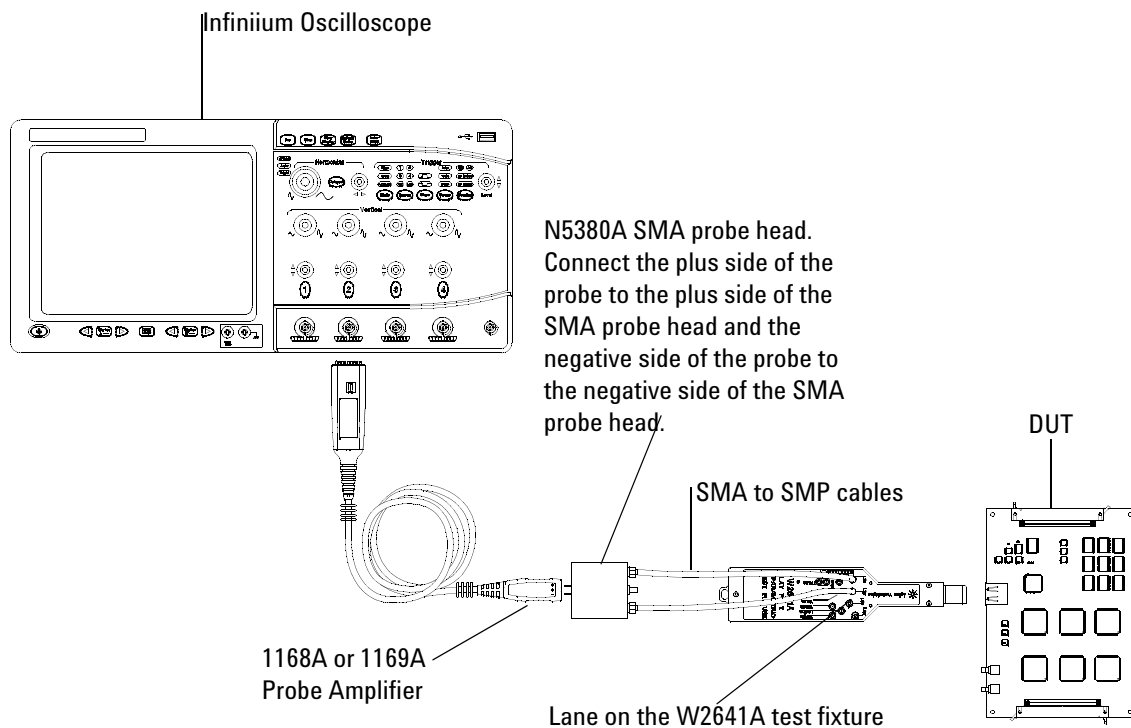


Figure 75 Probing for Differential Tests -Cable Non-ISI Jitter Tests (Single Connection with W2641A DisplayPort Test Fixture)

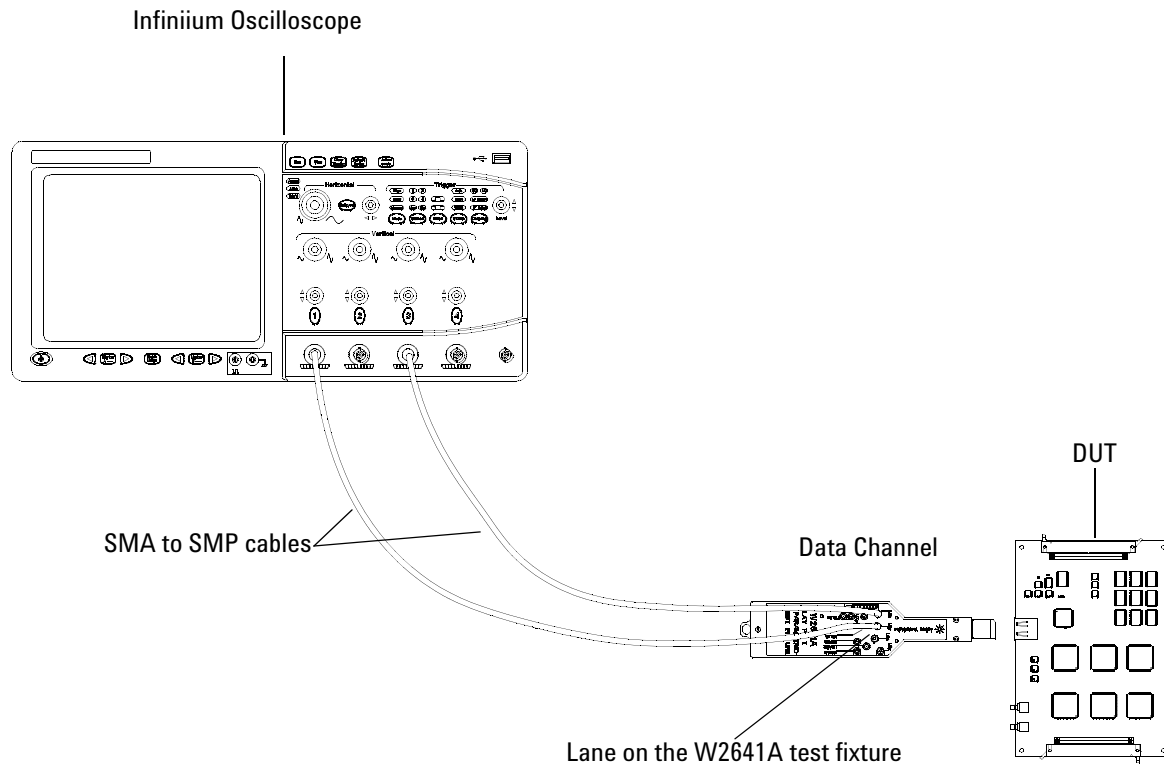


Figure 76 Differential Measurement Setup Using Two Single Ended Connections - Cable Non-ISI Jitter Tests (A Minus B Configuration)

You can use any oscilloscope channel and connect it to any lane test point. You select the channels used for testing lanes in the Set Up tab of the DisplayPort Electrical Performance Compliance Test Application.

The data lanes and channels shown in the previous figures are just examples. You can choose any desired data lane and channel that you want.

Cable Non-ISI Jitter Tests

To evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. (Reference: Table 3.13 VESA DisplayPort Standard).

The overall system jitter budget allocates different amounts of jitter which each component of the system is allowed to contribute. To exceed any of these limits is to violate the component level jitter budget. (Reference: Jitter model in base DisplayPort Specification (Section 3.5.3.9: The Dual Dirac Jitter Model)).

The test must use a PRBS 7 test pattern at all voltage levels. The test can be performed with pre-Emphasis for best performance results.

Test Procedure

- 1 Start the automated testing application as described in [“Starting the DisplayPort Electrical Performance Compliance Test Application”](#) on page 22.
- 2 Connect the W2641A test fixture or other appropriate fixture to the device under test (DUT).
- 3 If you are using one connection, connect the probe to one channel. If you are using two connections, connect the two probes to two channels of the oscilloscope. If you are using four connections, connect the four probes to four channels of the oscilloscope.
- 4 Connect the SMA to SMP cable to the SMA probe head of one of the probes and to the data lane connector on the W2641A fixture that you want to test.
- 5 Connect the other SMA to SMP cable to the other SMA probe head and to the data lane on the W2641A test fixture that you want to test.
- 6 In the DisplayPort Compliance Test Application, click the Set Up tab.
- 7 Set the DUT Definition Settings, Connection Type and Number of Channels according to the type of testing being done.

Navigate to the Non-ISI Jitter - Lane # - Non-ISI Jitter Test where # is the lane number to be tested.

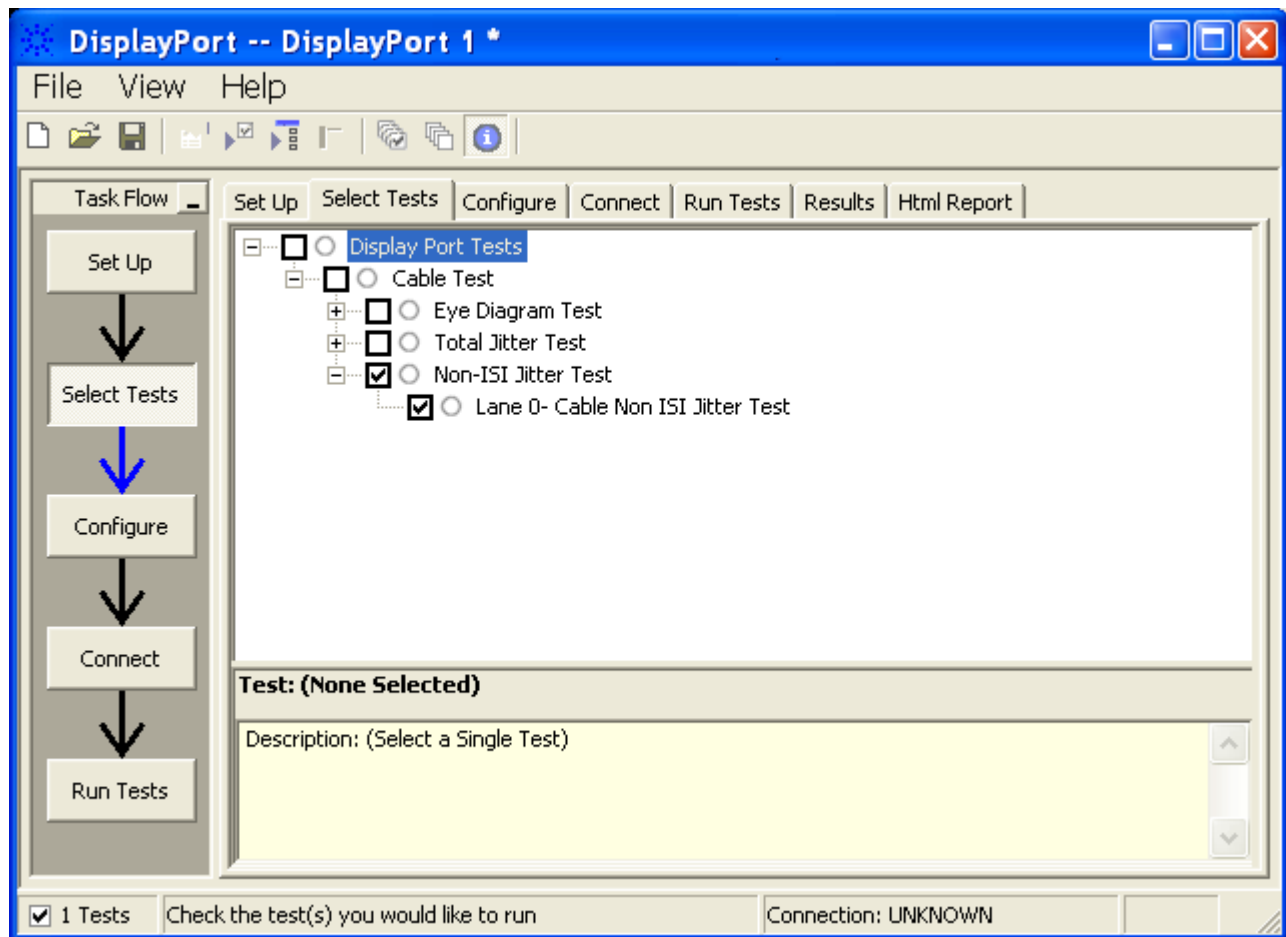


Figure 77 Selecting Cable Non-ISI Jitter Tests

- 8 Follow the DisplayPort Electrical Performance Compliance Test Application's task flow to set up configuration options (see [Table 28](#)), run the test and view the test results. Options may vary depending on selected mode: Compliance Mode or Debug Mode.

Table 28 Test Configuration Options

Configuration Option	Description
Clock Recovery Settings	
Clock Recovery Order	Set either a second order PLL or a first order PLL method to recover the clock.
Clock Recovery Loop Bandwidth (D10.2) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 1.62 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (D10.2) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when D10.2 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Loop Bandwidth (PRBS 7) - 2.7 Gbps	Sets the 3 dB bandwidth of the loop filter used by the PLL when PRBS 7 pattern is used. Please specify in correct format; xMHz, xkHz or xHz.
Clock Recovery Damping Factor	Sets the damping factor which is the value that used in designing the second order PLL to recover the clock. The damping factor and the 3 dB bandwidth of the PLL are related to the natural frequency using the following equation. $\omega_n = \frac{2\pi F_t}{\sqrt{2\zeta^2 - 1 + \sqrt{(2\zeta^2 - 1)^2 + 1}}}$ where: ω_n = the natural frequency of the PLL ζ = the damping factor of the PLL F_t = the 3 dB bandwidth of the PLL
Configurable Parameter Settings	
Bandwidth Reduction	Specifies the bandwidth frequency for the oscilloscope. This configuration is only available when the Enhanced Bandwidth or Noise Reduction option is installed on the oscilloscope.
Vswing Edge	Sets the number of Edges used when performing the Vswing measurement. The Vswing value is used to ensure that the waveform is displayed as large as possible in the waveform viewing area. Increasing this value increases the test run time but improves the repeatability of the measurement.
VTop & VBase Edge	Sets the number of edges required when making the VTop and VBase measurements.
Expert Mode	Turn on the expert mode for looser pre-requisite checker.

Table 28 Test Configuration Options

Configuration Option	Description
Test Plan Check Mode	Turn on test plan check mode to simulate the actual test plan run flow without actual tests being run.
SSC Acquisitions	Number of SSC cycle captured for SSC related tests. Maximum number is 25.
Low Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 1.62 Gbps.
High Bit Rate SSC Smoothing Points	Sets the number of smoothing points for SSC low pass filter when bit rate is 2.70 Gbps.
Memory Depth	Sets the memory depth for acquisition
Cable Test	
Cable Equalization	Selects the Type of Equalizer of the cable test.
Cable Construction	Selects the Cable Construction used.
Cable Mask	Selects the type of mask to use for the eye test.
Cable Mask Movement	This field contains 3 options. (1) Find Passing Mode will automatically search +/-0.5UI horizontally until no violation occurs, (2) Fixed Mask will not be moving, it only report Pass or Fail upon test, (3) Find Biggest Margin will search +/-0.5UI horizontally to find the maximum margin of non-violation mask.
Jitter Separation Edges	Sets the number of edges measured for the jitter separation test.
Bit Error Rate	Sets the bit error rate for the RJ/DJ measurements.

- 9 In order to perform the equalization, you have the option to use your own coefficient file. To do so, at the Configure page, under the Cable Equalizer option, Select “User Defined File” from the drop down menu.

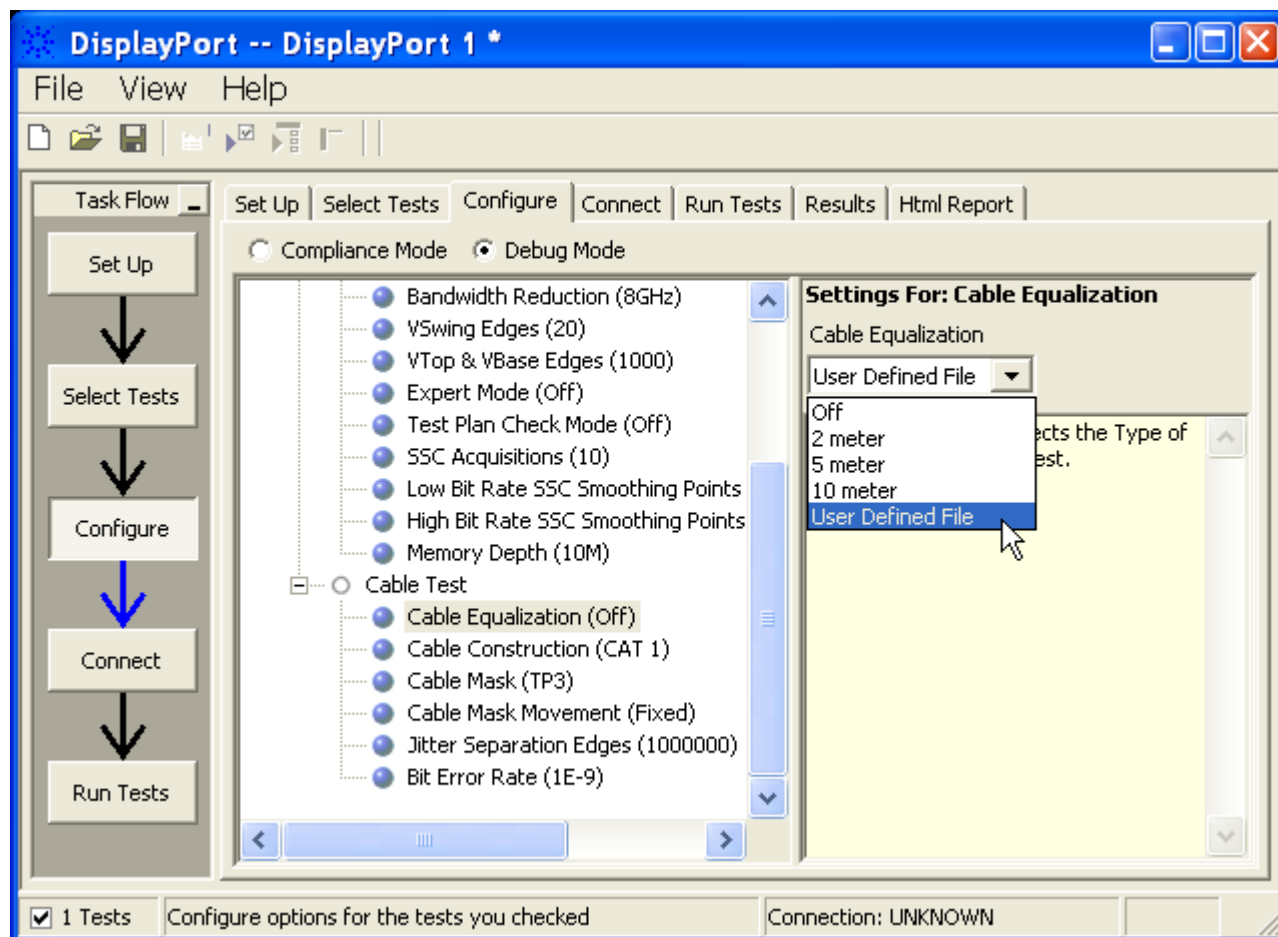


Figure 78 Selecting User Defined File for the Cable Equalizer

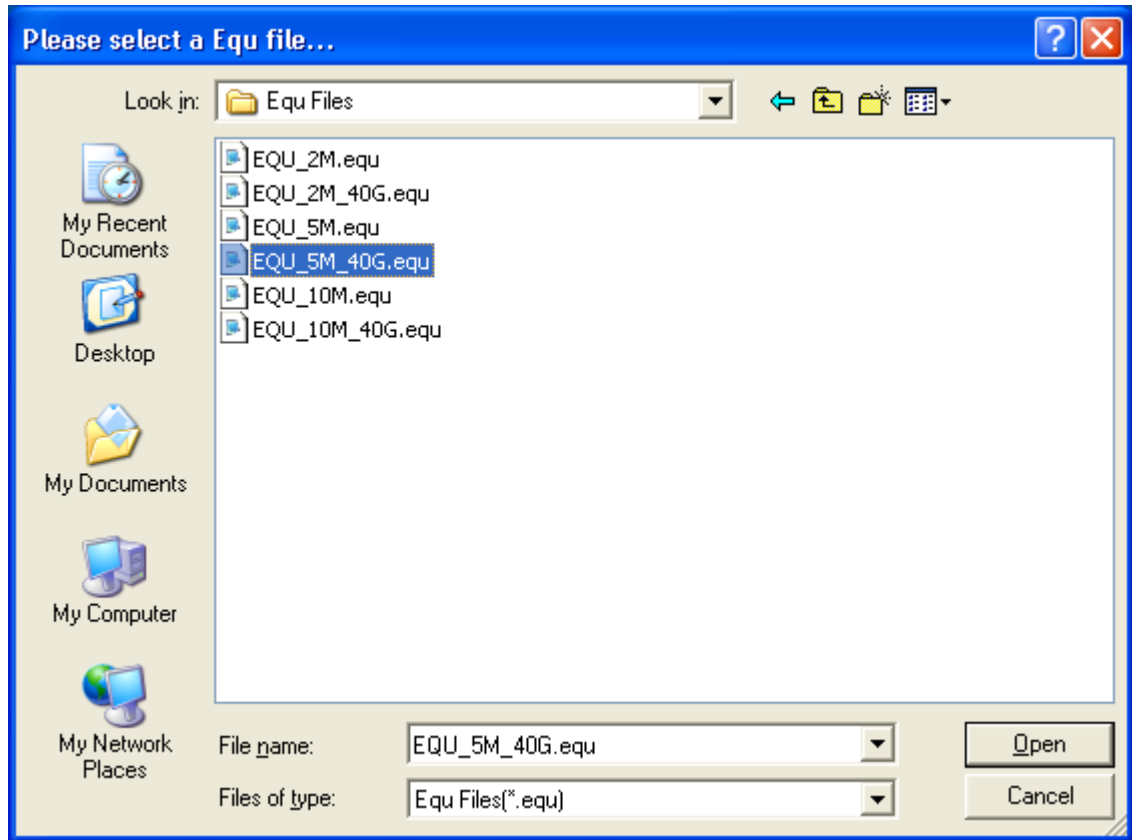


Figure 79 Selecting User Defined File

The following select file dialog box appears. Select your coefficient file (*.equ) and click Open. The test will run based on the your user defined coefficient file

PASS Condition

Table 29 Non-ISI Jitter at Internal and Compliance Points.

	Receiver package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.339 UI	0.330 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.465 UI	0.442 UI

UI is Unit Interval.

Test References

See Test 3.12: Non-ISI Jitter (TJ) Measurements in the
DisplayPort-Compliance Test Specification Version 1.



24 Calibrating the Infiniium Oscilloscope and Probe

Required Equipment for Calibration [214](#)

Internal Calibration [215](#)

Probe Calibration and De-skew [219](#)

This chapter describes the Agilent Infiniium digital storage oscilloscope calibration procedures.



Required Equipment for Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DisplayPort automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the Agilent Infiniium oscilloscopes).
- E2655A/B probe de-skew fixture.
- 82 Ω damping resistors (01130-81506) for the Socketed Differential Probe Head.

Figure 80 below shows a drawing of the above connector items.

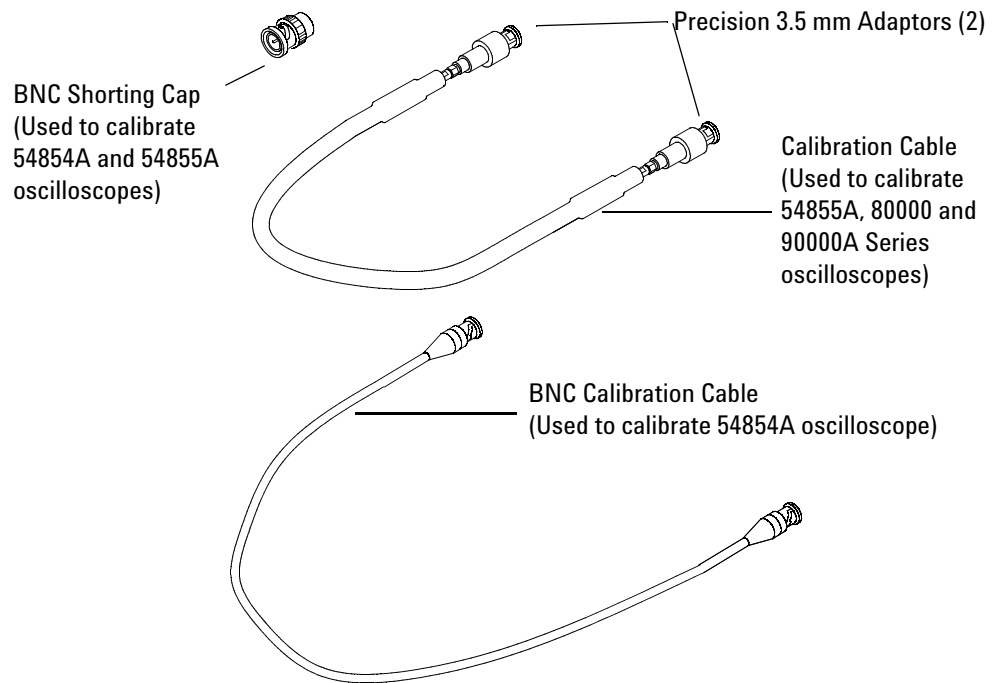


Figure 80 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

- 1 Set up the oscilloscope with the following steps:
 - a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.
 - b If a second monitor is being used, connect it to the VGA connector located near the LAN port, on the rear of the oscilloscope.
 - c Plug in the power cord.
 - d Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.
 - e Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 2 below.
- 2 Locate and prepare the accessories that will be required for the internal calibration
 - a Locate the calibration cable.
 - b Locate the two Agilent precision SMA/BNC adapters.
 - c Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.
 - d Attach the other SMA adapter to the other end of the calibration cable - hand tighten snugly.

- 3 Referring to [Figure 81](#) below, perform the following steps:
 - a Click on the **Utilities>Calibration** menu to open the Calibration window.

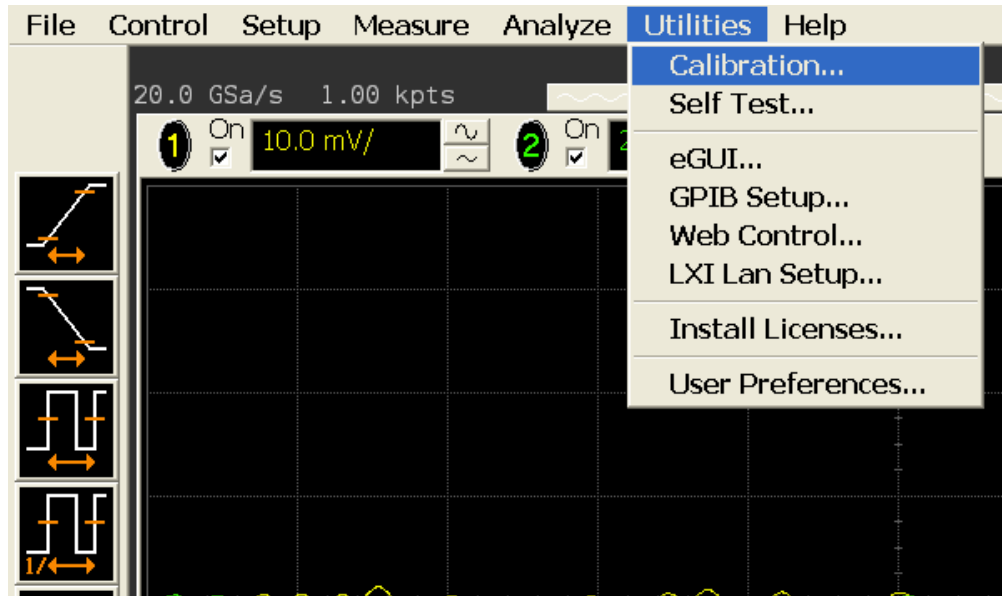


Figure 81 Accessing the Calibration Menu.

- 4 Referring to [Figure 82](#) below, perform the following steps to start the calibration:
 - a Uncheck the Cal Memory Protect checkbox.
 - b Click the Start button to begin the calibration.

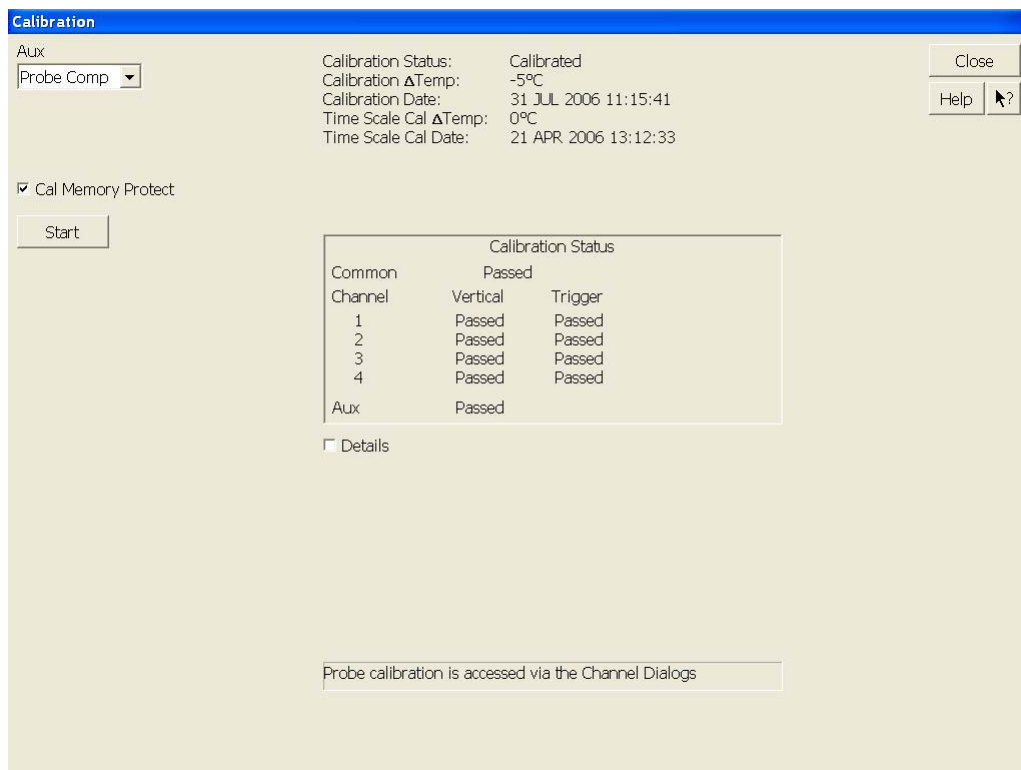


Figure 82 Oscilloscope Calibration Window

5 Follow the on-screen instructions:

- a** You will be prompted to disconnect everything from all the inputs: click the OK button.
- b** Then you will be prompted to connect the calibration cable with SMA adapters between the Aux Out and a specified input. Install the SMA adapter by pressing it on input BNC, and hand tightening the outer ring turning right. Click the OK button after connecting the cable as prompted.
- c** During the calibration of channel 1, you will be prompted a Calibration Options screen, as shown in [Figure 83](#) below.

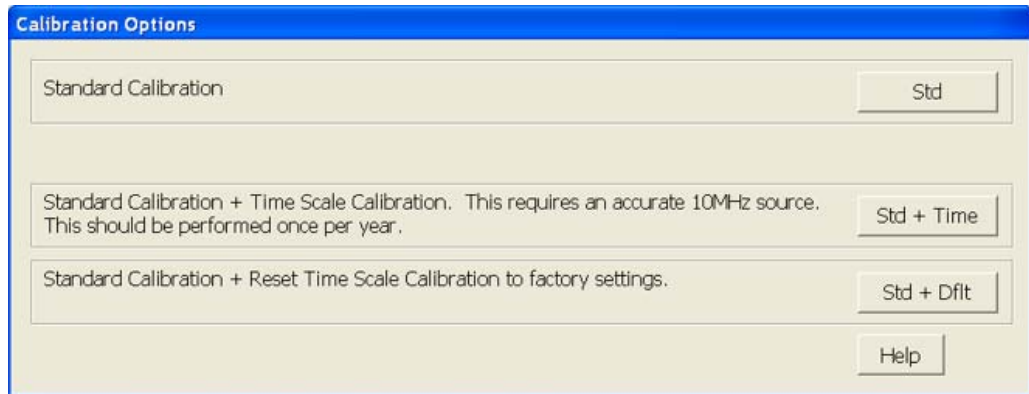


Figure 83 Time Scale Calibration Dialog box

- d** Click on the Std + Dflt button to continue the calibration, using the Factory default calibration factors.
- e** When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.
- f** Confirm that the Vertical and Trigger Calibration Status for all Channels passed.
- g** Click the Close button to close the calibration window.
- h** The internal calibration is completed.
- i** Read NOTE below.

NOTE

These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Probe Calibration and De-skew

Before performing DisplayPort tests you should calibrate and de-skew the probes.

SMA probe head Atten/Offset Calibration

- 1 Referring to [Figure 84](#) below, perform the following steps:
 - a Ensure that a probe, attached with SMA probe head is connected to Channel 1. Install the 82 Ω resistors into the SMA probe head. Connect the de-skew fixture to Aux Out. Clip the resistors on de-skew fixture. These resistors are only required for probe calibration and de-skew.
 - b Click on the **Setup>Channel 1** menu to open the Channel Setup window.

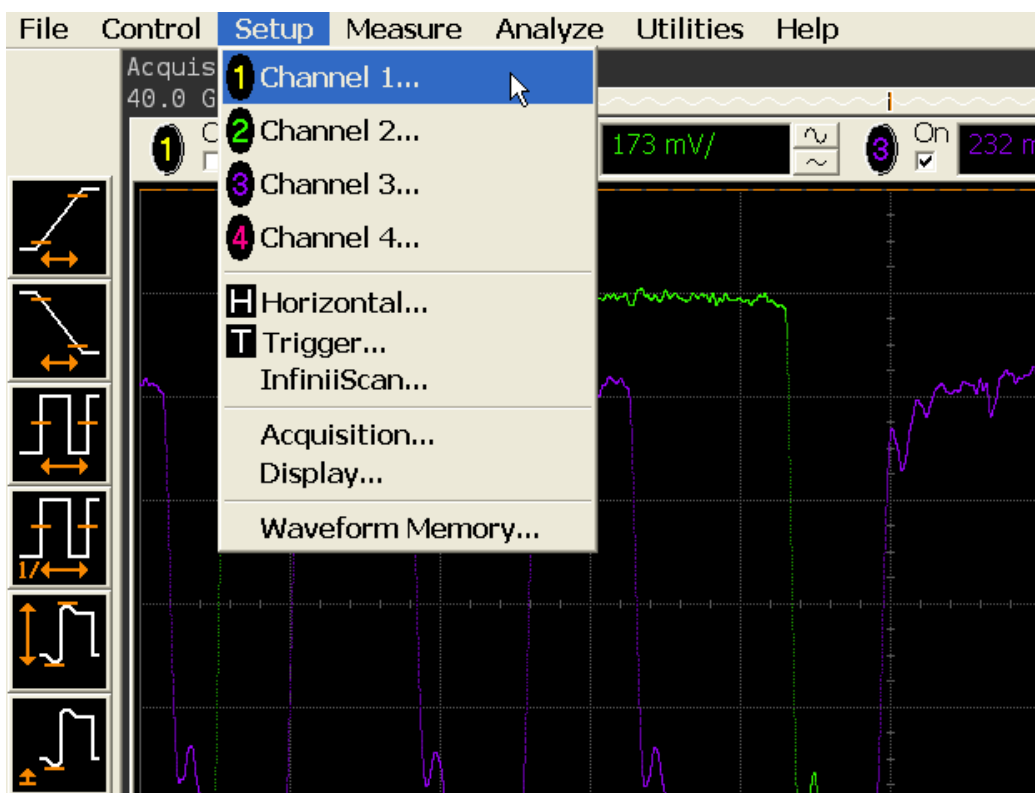


Figure 84 Channel Setup Window.

- c Click the Probes button in the Channel Setup window, to open the Probe Setup window.

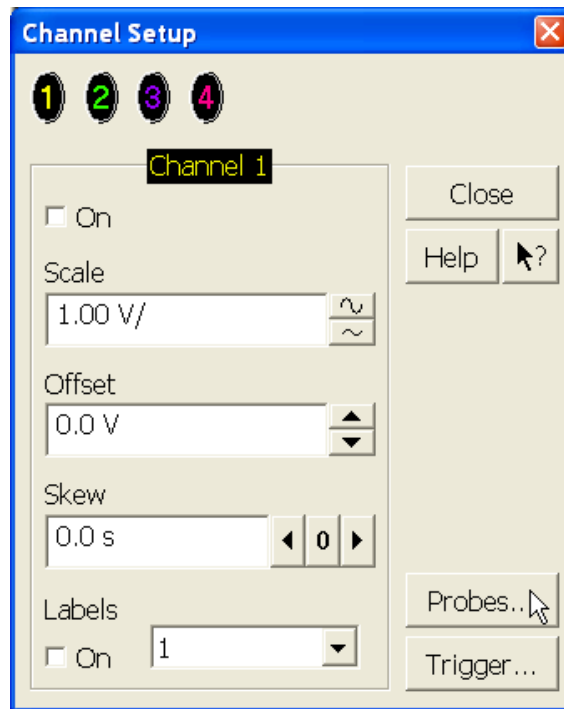


Figure 85 Channel Dialog Box

- 2 Referring to [Figure 86](#) below, perform the following steps:
 - a Click the Add Head... button, and then select E2678A:DF Sckt from the list of Head Type. Select OK to close the dialog box.

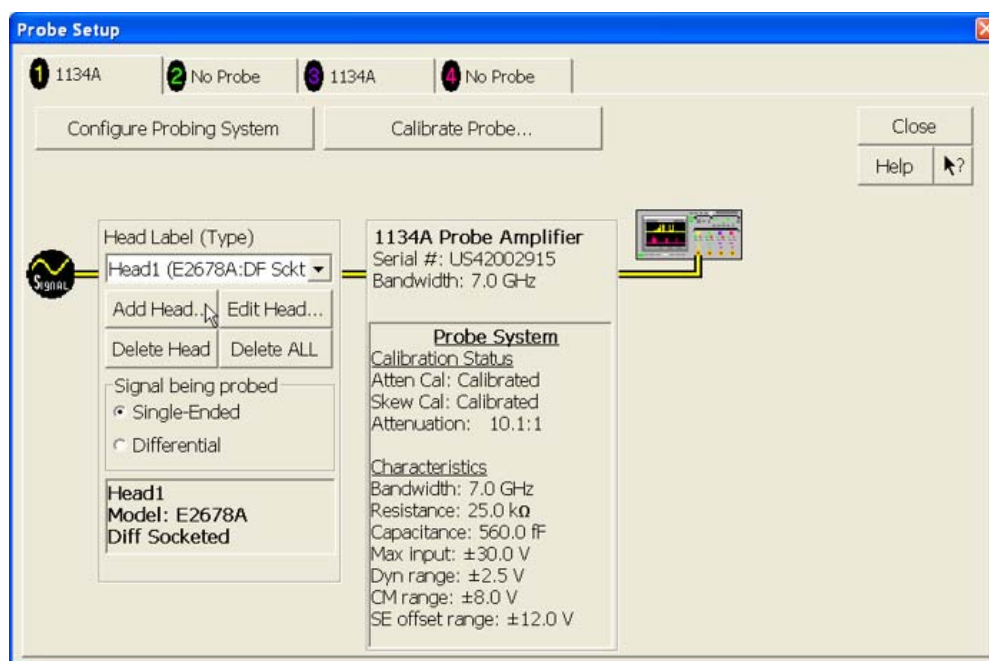


Figure 86 Probe Setup Window.

- 3 Referring to [Figure 87](#) below, perform the following steps:
 - a Click on the Calibrate Probe button to open the Probe Calibration window.

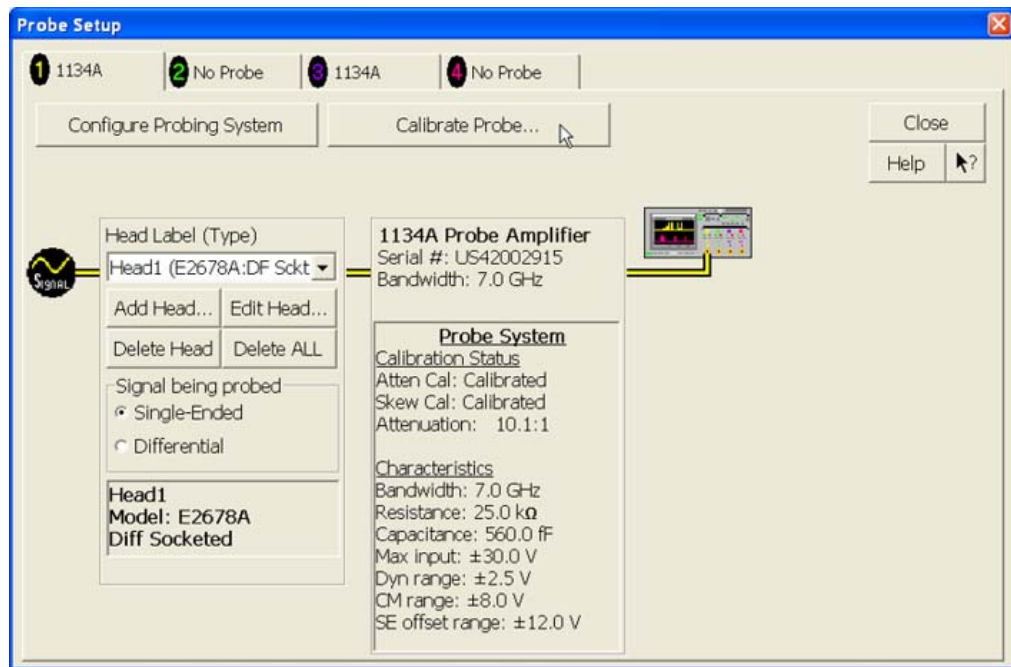


Figure 87 User Defined Probe Window.

- 4 Referring to [Figure 88](#) and perform the following steps:
 - a Select the Calibrated Atten/Offset Radio Button
 - b Click the Start Atten/Offset Calibration Button to open the Calibration window.

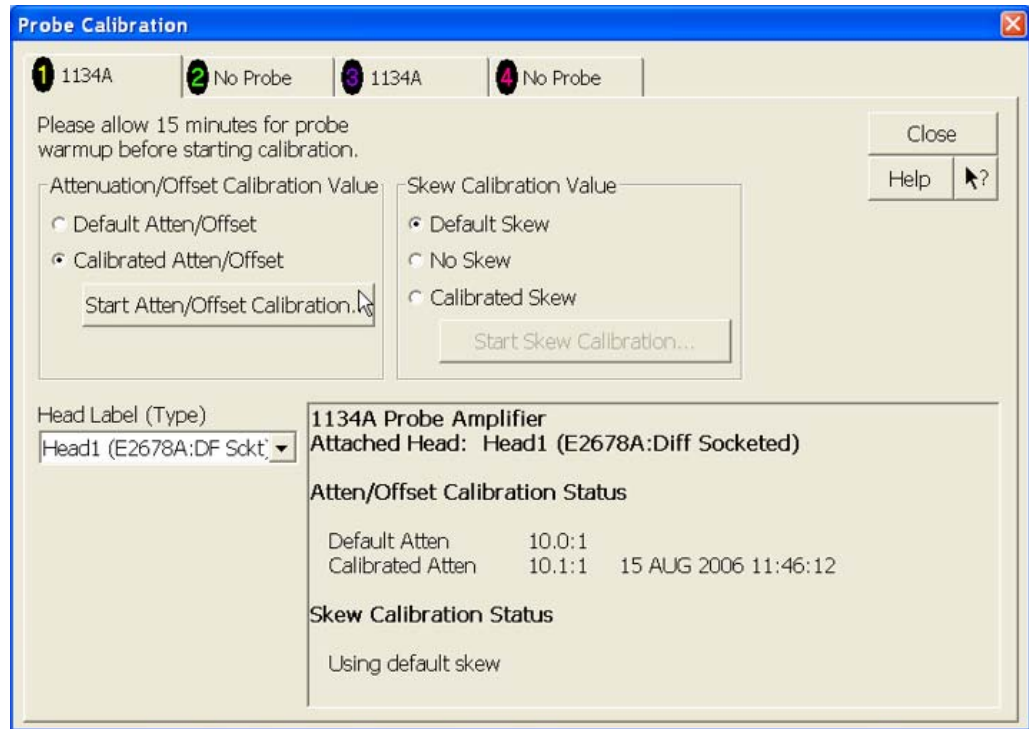


Figure 88 Probe Calibration Window.

- c Follow the on-screen instructions.
- d At the end of the Atten/Offset Calibration perform the Skew Calibration.

Differential Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

- 1 Referring to [Figure 89](#) below, perform the following steps:
 - a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

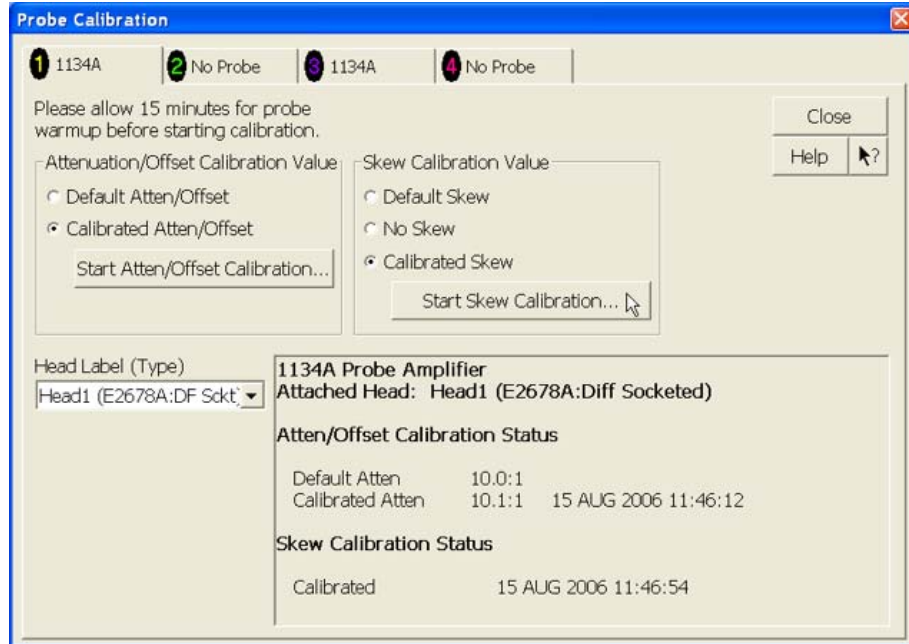


Figure 89 De-skew Connection.

NOTE

Each probe is calibrated to the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes are labeled with the channel on which they were calibrated.

SMA Probe Head Atten/Offset Calibration

- 1 Referring to [Figure 90](#) below, perform the following steps:
 - a Connect the SMA to BNC adaptor to one of the SMA connectors of the deskew fixture or SMA (f) to SMA (f) adapter.
 - b Connect the 50 ohm terminator to the center SMA connector of the SMA probe head.
 - c Connect the other end of the deskew fixture or SMA (f) to SMA (f) adapter to one of the SMA connectors of the SMA probe head.
 - d Connect the BNC connector of the SMA to BNC adaptor to the Aux Out on the front panel of the Infiniium oscilloscope.
 - e Connect the positive (+) side of the InfiniiMax probe amp to the GPO (SMP) connector of the SMA probe head whose path is connected to

the Aux Out of the oscilloscope. Do not connect the negative (-) side of the InfiniiMax probe amp to anything.



Figure 90 SMA Probe Head Calibration

- f Click on the **Setup>Channel 1** menu to open the Channel Setup window.

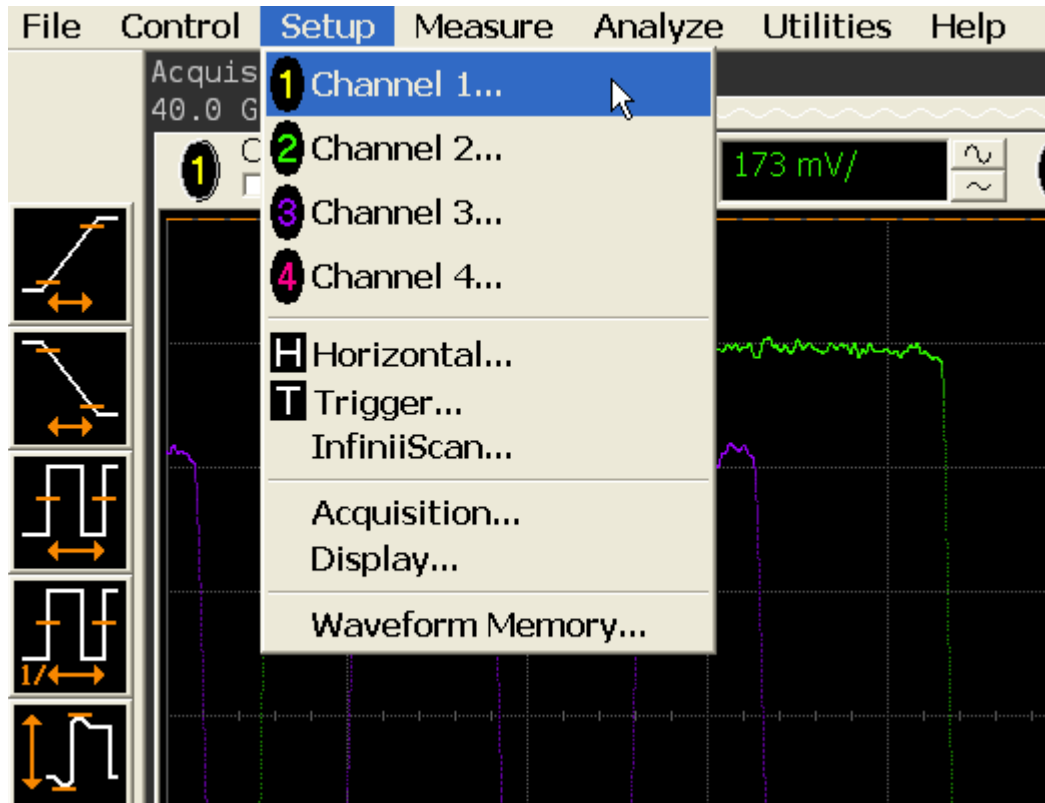


Figure 91 Channel Setup Window

- g Click the Probes button in the Channel Setup window, to open the Probe Setup window.

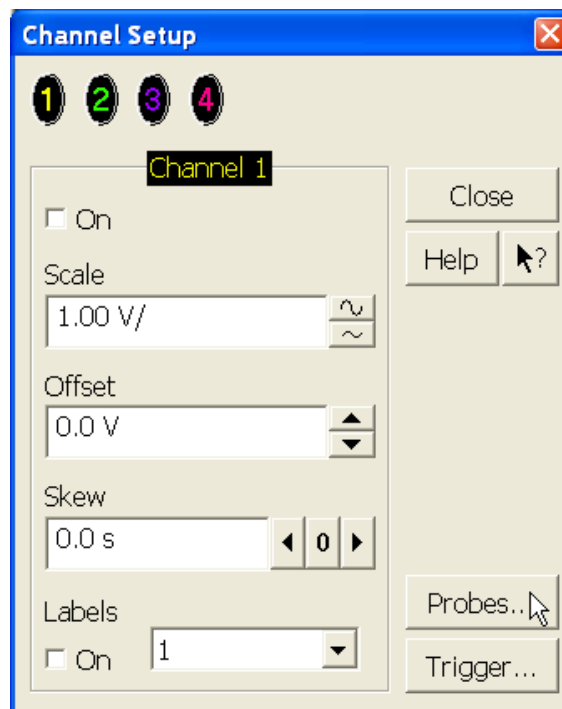


Figure 92 Channel Dialog Box

- 2 Referring to [Figure 93](#) below, perform the following steps:
 - a Click the Add Head... button, and then select N5380A:DF SMA from the list of Head Type. Select OK to close the dialog box.

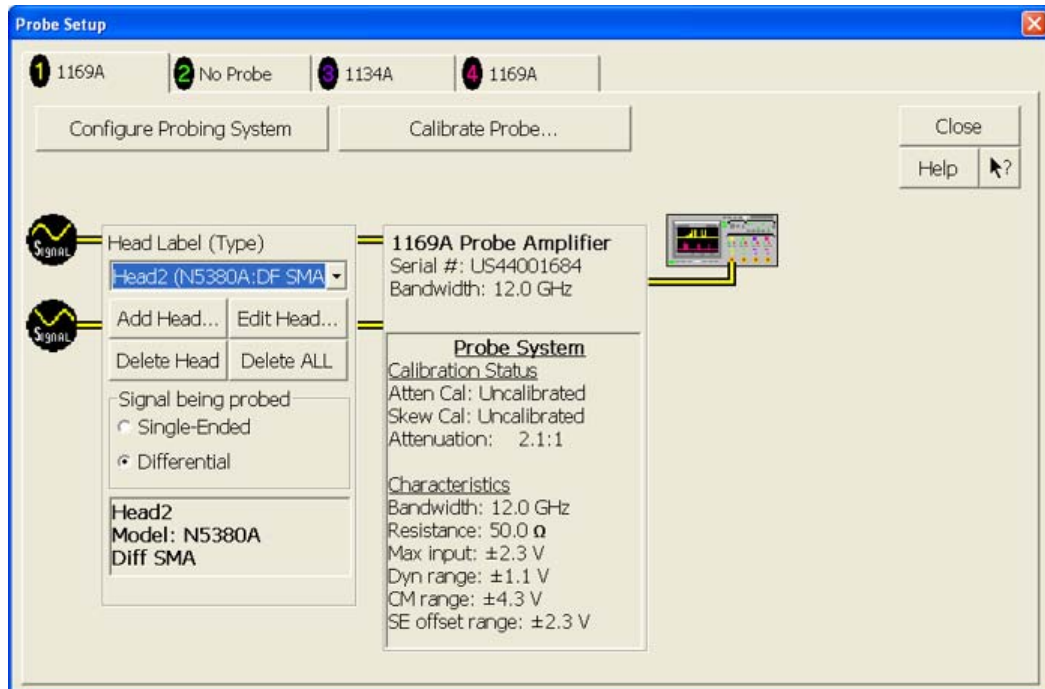


Figure 93 Probe Setup Window.

- b Click on the Calibrate Probe button to open the Probe Calibration window.
- 3 Referring to [Figure 94](#) below, perform the following steps:
 - a Select the Calibrated Atten/Offset Radio Button
 - b Click the Start Atten/Offset Calibration Button to open the Calibration window.

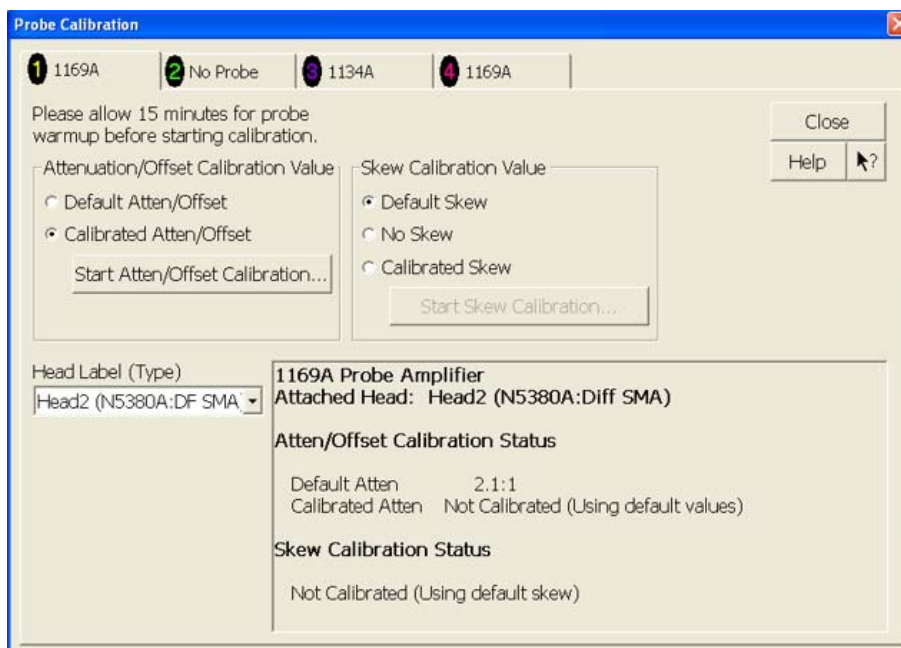


Figure 94 Probe Calibration Window.

- c Follow the on-screen instructions.
- d At the end of the Atten/Offset Calibration perform the Skew Calibration.

SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. Perform the following steps:

- 1 Referring to [Figure 95](#) below, perform the following steps:
 - a Select the Start Skew Calibration button and follow the on-screen instructions. For more information on proper connection of probe to the oscilloscope, refer to the De-skew and Calibration manual. This

manual comes together with the E2655A/B De-skew Kit, that came with your oscilloscope.

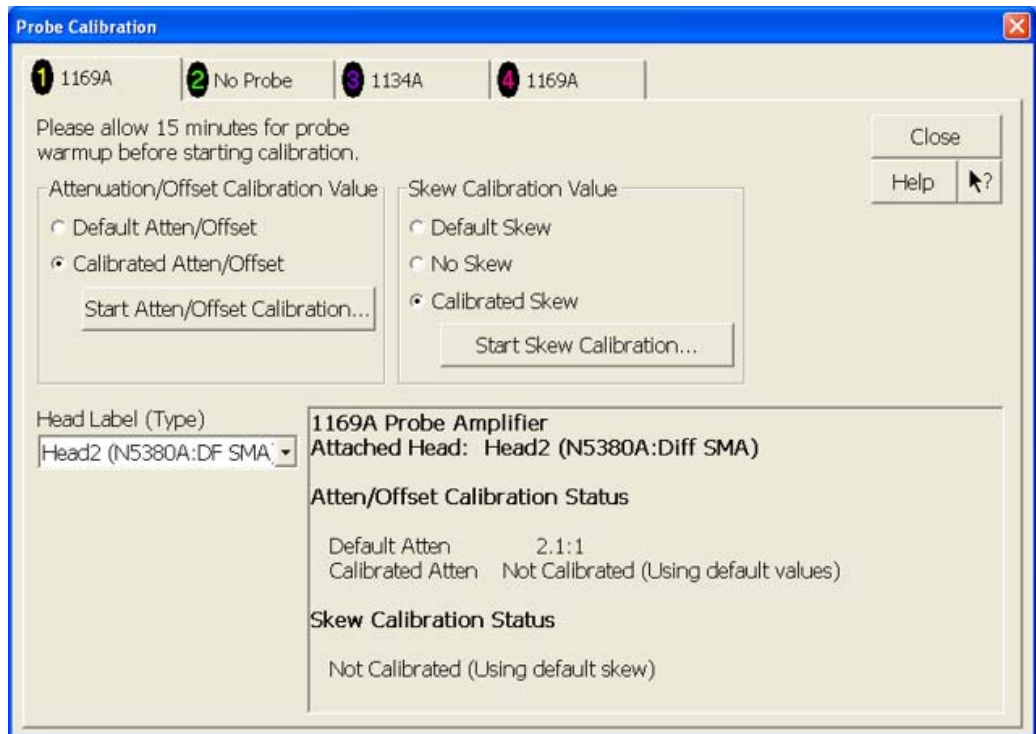
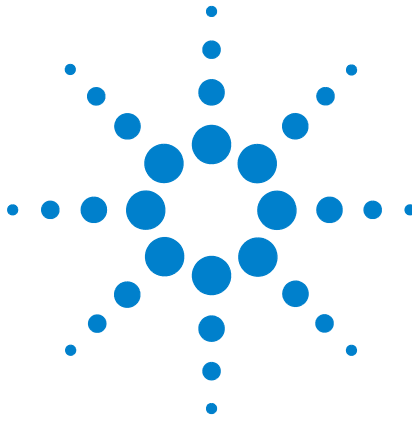


Figure 95 De-skew Connection.



25 InfiniiMax Probing



Figure 96 1169A InfiniiMax Probe Amplifier

Agilent recommends the N5380A SMA probe head and the N5380A differential SMA probe head.



Figure 97 Recommended Socketed Probe Head for the DisplayPort Testing

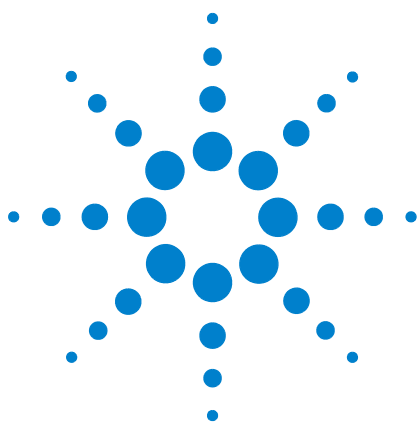


Figure 98 Recommended SMA Probe Head for DisplayPort Testing



Table 30 Probe Head Characteristics

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential socket	E2678A	7 GHz, 0.34 pF, 50 kOhm	7 GHz, 0.56 pF, 25 kOhm
Hi-BW differential SMA	N5380A	12 GHz	12 GHz



A DisplayPort Source Automated Test with W2642A DPTC

Aux Channel and Hot Plug Detect (HPD) [234](#)

DPTC Controller [235](#)

Automated Test Sequence [236](#)

This section describes the implementation of the test automation features architect in the *DisplayPort Standard Version 1.1a*. The Automated DisplayPort Test requires a source device to be able to change the test conditions such as data rate, level, pre-Emphasis, test pattern and SSC option as requested. This section provides a guide on how to perform these tasks using a sink emulator such as Agilent W2642A DisplayPort Test Controller (DPTC).



Aux Channel and Hot Plug Detect (HPD)

DisplayPort devices communicate with each other through the aux channel. The DisplayPort sink device provides memory where a source and a sink could read/write into this memory. *DisplayPort Standard 1.1a* has reserved a set of DCPD registers for the purpose of test automation.

There is a HPD line between a source and a sink too. For automation purpose, the HPD pulse is used as an IRQ to notify the source about a test automated request.

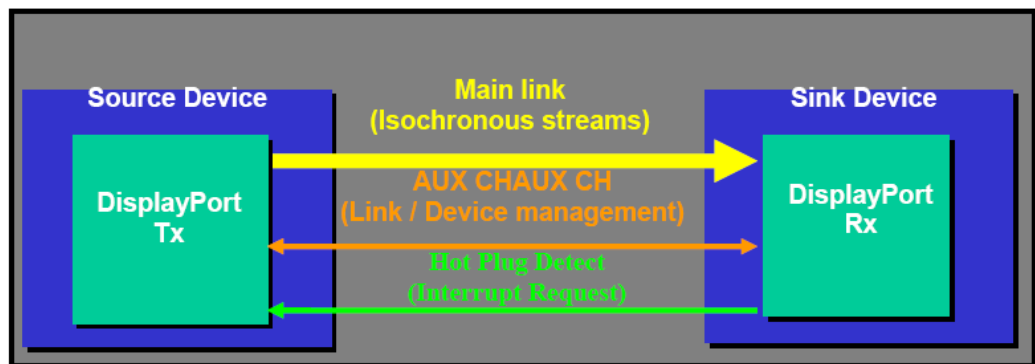


Figure 99 Communication between the Source Device and Sink Device

DPTC Controller

The Agilent W2642A DPTC can be used as a sink emulator to communicate with the source to output the desired signals. Some fundamental functions provided to enable automation are:

- SetByte(Address, Value)
- Send HPDPulse(Length)
- PlugIn(Emulate Plug in event)
- PlugOut(Emulate Plug out event)

NOTE

The above listed function names for informative purpose only. They do not reflect the actual API call.

Automated Test Sequence

This section provides information on how to enable the test automation in DisplayPort Source test. You should specify the max link rate, lane count, preEmphasis, Level and SSC option in the compliance application.

OPTION 1

Step 1: Emulate successful link training (For SSC)

- 1 This step emulates a fake link training to cheat the source that a sink device is connected.
- 2 To do this, the DPTC controller initiates the sequence as below:
 - a Emulate PlugOut Event to put HPD line in Low for at least 2ms. Source should RESET
 - b Set Link Capability fields as below:
 - MAX_LINK_RATE = 0x0A
 - MAX_LANE_COUNT = 0x04
 - MAX_DOWNSPREAD = 0x01 to enable SSC / 0x00 to disable SSC
 - c Set 0x202 (LANE0_1_STATUS) = 0x77
 - d Set 0x203 (LANE2_3_STATUS) = 0x77
 - e Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81
 - f Emulate PlugIn Event to put HPD line in High
 - g Source clears Link Configuration field and reads Link Capability
 - h Source enables or disables SSC based on the value of MAX_DOWNSPREAD (Enable SSC if value is 1) and writes to DOWNS_SPREAD_CTRL. Source writes LINK_BW_SET, TRAINING_LANE[X,Y]_SET, LANE_COUNT_SET based on default settings
 - i Source outputs 0x01 to TRAINING_PATTERN_SET
 - j Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Since these registers are already set in step 3-5, source exits the Clock Recovery Sequence of Link Training (Figure 100) and go to Channel Equalizer sequence for Link Training (Figure 101).
 - k Source sets TRAINING_PATTERN_SET to 0x02.
 - l Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Since these registers are already set in step 3-5, source exits Channel Equalizer sequence and ends the entire link training process.

- 3 This sequence cheats the DisplayPort source that the link training has already been performed without looping through the actual link training. As such, the DisplayPort source device exits the link training successfully.
- 4 Aux Controller checks DOWNS_SPREAD_CTRL if SSC support has changed.

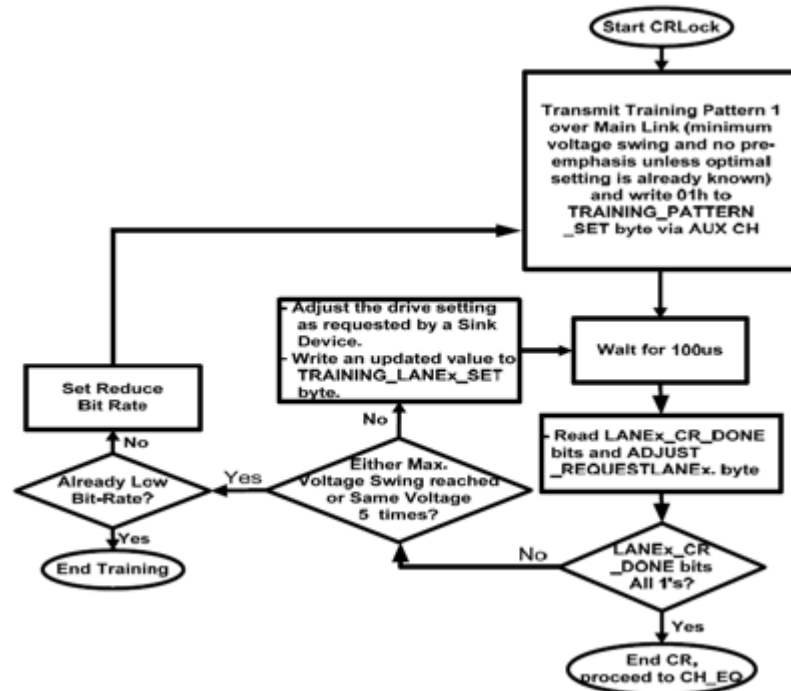


Figure 100 Clock Recovery Sequence of Link Training

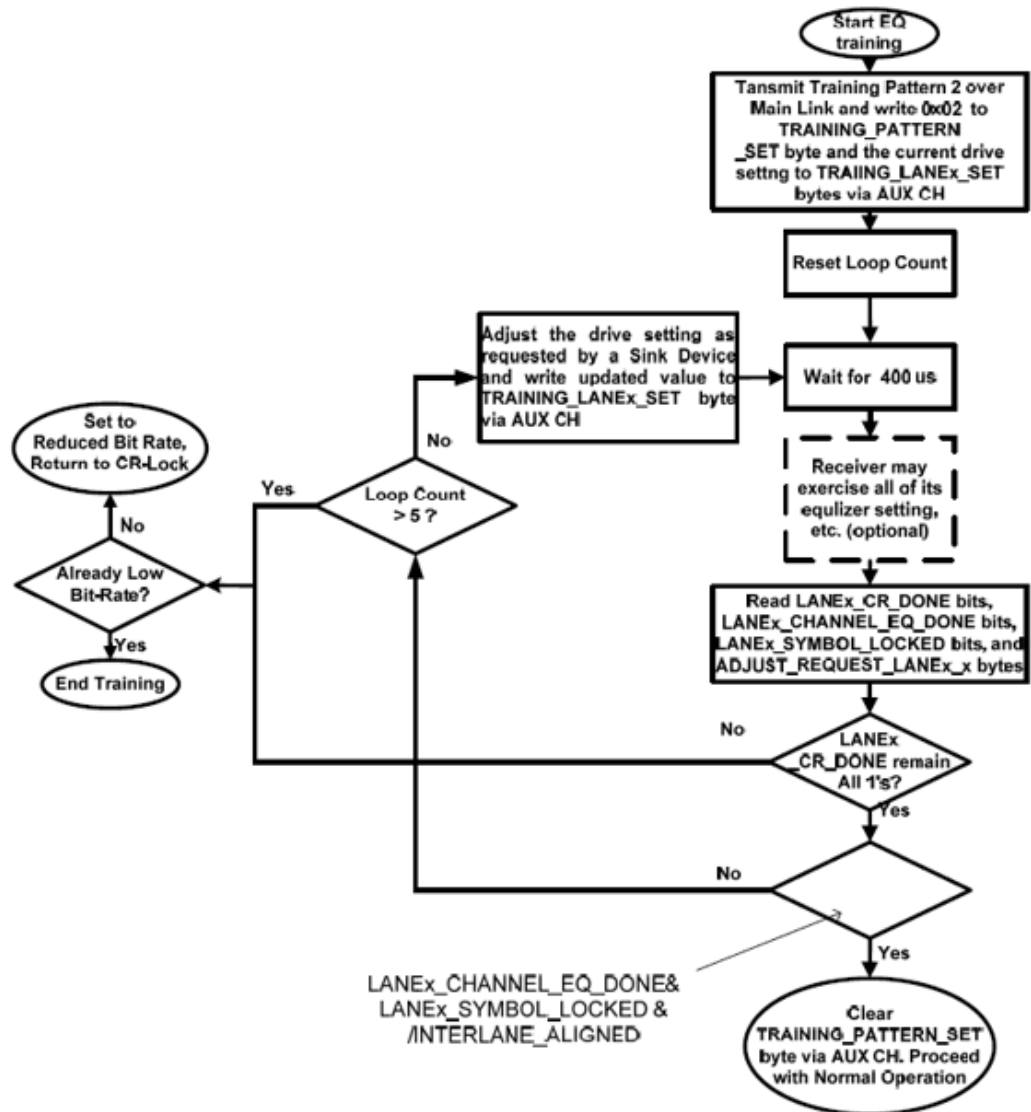


Figure 101 Channel Equalization Sequence of Link Training

Step2: Change Bit Rate and Number of Lanes

- 1 To change the bit rate and number of lanes, DPTC controller will initiate the below sequence:
 - a Set 0x202 (LANE0_1_STATUS) = 0x77
 - b Set 0x203 (LANE2_3_STATUS) = 0x77
 - c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81
 - d Set bit 0x201.1 (AUTOMATED_TEST_REQUEST)
 - e Clear 0x218(TEST_REQUEST)
 - f Set bit 0x218.0 (TEST_LINK_TRAINING)
 - g Set byte 0x219 (TEST_LINK_RATE) to 0x0A(2.7 Gbps) or 0x06(1.62 Gbps)
 - h Set byte 0x220 (TEST_LANE_COUNT) to desired lane count
 - i Trigger an IRQ Event(Send 1ms HPD Pulse)
- 2 Once a 1ms HPD pulse is received:
 - a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted, go to 2
 - b If 0x218.0 is asserted, source clears LINK_BW_SET and LANE_COUNT_SET
 - c Source reads 0x219 and 0x220 and outputs signals with desired lane count and data rate
 - d Source writes new values to LINK_BW_SET, LANE_COUNT_SET.
 - e Source clears bit 218.0 if a DisplayPort source successfully outputs signals with desired lane count and data rate
- 3 Aux Controller checks LINK_BW_SET, LANE_COUNT_SET if signal change is successful.

Step3: Change Pre-Emphasis, Level and Test pattern

- 1 To change the pre-Emphasis, level and test pattern, DPTC initiates the following sequences:
 - a Set 0x202 (LANE0_1_STATUS) = 0x77
 - b Set 0x203 (LANE2_3_STATUS) = 0x77
 - c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81
 - d Set bit 0x201.1 (AUTOMATED_TEST_REQUEST)
 - e Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with the desired level and pre-Emphasis

Table 31 Mapping Table for Pre-Emphasis and Level

VOLTAGE_SWING_LANEX (2 bits)
00: 400 mV
01: 600 mV
10: 800 mV
11: 1200 mV

Table 32 Mapping Table for Pre-Emphasis and Level

PRE-EMPHASIS_SWINT_LANEX (2 bits)
00: 0 dB
01: 3.5 dB
10: 6 dB
11: 9.5 dB

f Clear 0x218 and Set bit 0x218.3(TEST_PATTERN_REQUEST)

g Set 0x248(PHY_TEST_PATTERN) to the desired pattern

Table 33 Physical Test Pattern Required

Bits 1:0 = PHY_TEST_PATTERN_SEL
00: No test pattern selected
01: D10.2 without scrambling
10: Symbol_Error_Measurement_Control
11: PRBS7

h Send IRQ to source(HPD 1ms Pulse)

- 2 Once a 1ms HPD pulse is received:
 - a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted, go to step 2
 - b If 0x218.3 is asserted, source clears TRAINING_LANE[X,Y]_SET, TRAININ_PATTERN_SET:LINK_QUAL_PATTERN_SET
 - c Source reads 0x248,0x206,0x207 and outputs signals with the desired pattern, Pre-Emphasis and level
 - d Source updates TRAINING_LANE[X,Y]_SET, TRAININ_PATTERN_SET:LINK_QUAL_PATTERN_SET
 - e If successful, source clears bit 218.3
 - f If the test request is successful, sink checks TRAINING_LANE[X,Y]_SET, TRAININ_PATTERN_SET:LINK_QUAL_PATTERN_SET

OPTION 2

This option provides an easier way to control the test automation in one simple step. However, it is less consistent with the DisplayPort Automation scheme.

Step 1:

- 1 Source should always scan for 0x201.1 (AUTOMATED_TEST_REQUEST).
- 2 Sink sets the following:
 - a Set byte 0x219 (TEST_LINK_RATE) to 0x0A(2.7 Gbps) or 0x06(1.62 Gbps)
 - b Set bit 0x03.1(TEST_DOWNSPREAD) to turn on SSC. Clear 0x21A.1 to turn off SSC
 - c Set byte 0x220 (TEST_LANE_COUNT) to desired lane count
 - d Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with desired level and preemphasis
 - e Set 0x248(PHY_TEST_PATTERN) to desired pattern
- 3 Sink sets 0x201.1.
- 4 Once source detects 0x201.1 being set, it outputs signals as in step 2, as a response.
- 5 Source sets bit 0x218.0 to indicate that the operation is completed.
- 6 Sink sets bit 0x218.0 back to 0.
- 7 Alternatively, HPD_IRQ(1ms) mechanism could be used instead of scanning 0x201.1

A DisplayPort Source Automated Test with W2642A DPTC

Index

A

AC common mode noise tests, 137

B

BNC to SMA male adapter, 4, 214

C

cable eye diagram tests, 183
cable non-ISI jitter tests, 203
cable total jitter tests, 193
calibrating the oscilloscope, 213
calibration cable, 4, 214
configure, 23
connect, 23

D

DisplayPort automated testing—at a glance, 3

H

HTML report, 23

I

in this book, 5
inter pair skew tests, 87
internal calibration, 215
intra pair skew tests, 129

K

keyboard, 3, 214

L

license key, installing, 17
link layer protocol tests, 145

M

main link frequency compliance tests, 103
mouse, 3, 214

N

non pre-Emphasis level tests, 61

O

overshoot tests, 69

P

precision 3.5 mm BNC to SMA male adapter, 4, 214
pre-Emphasis level tests, 77
probe calibration, 219, 224, 229
probing for AC common mode noise tests, 138
probing for cable eye diagram tests, 184
probing for cable non-ISI jitter tests, 204
probing for cable total jitter tests, 194
probing for inter pair skew tests, 88
probing for intra pair skew tests, 130
probing for link layer tests, 146
probing for main link frequency compliance tests, 104
probing for non pre-Emphasis level tests, 62
probing for overshoot tests, 70
probing for pre-Emphasis level tests, 78
probing for rise-fall mismatch tests, 122
probing for sink eye diagram tests, 154
probing for sink non-ISI jitter tests, 174
probing for sink total jitter tests, 164
probing for source data eye diagram tests, 26
probing for source non-ISI jitter tests, 46
probing for source total jitter tests, 38
probing for spread spectrum clocking (ssc) differential tests, 112
probing for transition time tests, 54
probing for unit interval tests, 96

R

report, 23
required equipment and software, 3
required equipment for calibration, 214
results, 23
rise and fall time mismatch tests, 121
run tests, 23

S

select tests, 23
sink eye diagram tests, 153
sink non-ISI jitter tests, 173
sink total jitter tests, 163
source eye diagram tests, 25
source non-ISI jitter tests, 45
source total jitter tests, 37

spread spectrum clocking (ssc) tests, 111
starting the DisplayPort automated test application, 22

T

transition time tests, 53

U

U7232A DisplayPort Electrical Performance Compliance Test Application, 3
unit interval tests, 95

www.agilent.com

© Agilent Technologies, Inc. 2007-2009

Fifth edition, March 2009
This part is not orderable.

U7232-97004



Agilent Technologies